

Circuit Self-Recovery Experiments in Extreme Environments

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Abstract

Temperature and radiation tolerant electronics, as well as long life survivability are key capabilities required for future NASA missions. Current approaches to electronics for extreme environments focus on component level robustness and hardening. However, current technology can only ensure very limited lifetime in extreme environments. This paper describes novel experiments that allow adaptive in-situ circuit redesign/reconfiguration in extreme temperature and radiation environments. This technology would complement material/device/layout advancements and increase the mission capability to survive harsh environments. The approach is demonstrated on a mixed-signal programmable chip (FPTA-2), which recovers functionality for temperatures reaching 280°C and with total radiation dose up to 175kRad.

1. Introduction

Long-life space missions and extreme environments have characteristics such as high radiation level (Europa Surface and Subsurface mission, 5 MRad), high temperature (Venus Surface Exploration and Sample Return mission, 460°C) and low temperature (Titan in-situ mission, -180°C). Such missions and environments have dictated the need for new electronics technologies.

Material and circuit solutions have been employed for high temperature environments. Materials used up to 300°C include bulk silicon and silicon-on-insulator (SOI) technologies; for higher

temperatures, gallium arsenide (GaAs), silicon carbide (SiC), and diamond show promise, and devices have been demonstrated at 500°C. Circuit solutions that compensate offset voltage and current leakage problems are described for example in [1].

Electrons and protons in space can also cause permanent damage in electronic devices that can lead to operational failure. Particularly, Single Event Effects (SEE) are radiation induced errors in microelectronic circuits caused when charged particles lose energy by ionizing the medium through which they pass. One technique for environments with high levels of radiation is the use of Radiation Hard technologies such as Silicon on Insulator (SOI), which allows compensating for the effect of radiation. However, the fabrication cost associated with extreme environment electronics is high.

In this paper we will present another technique, based on Evolvable Hardware, for electronic survivability in high temperature and radiation environments. A reconfigurable chip developed at JPL, the Field Programmable Transistor Array (FPTA-2) chip, is used in the experiments described in this paper. We submitted this chip to high temperature and radiation using JPL facilities. We show that the correct functionality of some circuits, such as half-wave rectifiers and low-pass filters, can be recovered using Evolutionary Algorithms. The Evolutionary Algorithms control the state of about 1,500 switches. Using a population of about 500 candidates and after running the Evolutionary process for about 200 generations, the correct functionality is recovered.

The rest of this paper is structured as follows: Section 2 reviews the Evolvable System. Section 3 describes the testbeds used during high temperature and radiation tests. Section 4 describes the results obtained. Finally, the main conclusions of the work are listed in section 5.

2. Evolvable System

A complete stand-alone board-level evolvable system (SABLES) is built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm [2]. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature and radiation experiments. The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 individuals from 100 to 200 generations require only 20 seconds.

The FPTA is an evolution-oriented reconfigurable architecture (EORA). It has a configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits.

The architecture of the FPTA consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The re-configurable

circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, C_{m1} , C_{m2} and C_c , of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors.

3. Experimental Testbeds

A high temperature testbed was built to achieve temperatures exceeding 350°C on the die of the FPTA-2 while staying below 280°C on the package. It is necessary to stay below 280°C on the package in order not to destroy the interconnects and package integrity. Die temperatures should stay below 400°C to make sure die attach epoxy does not soften and that the crystal structure of the aluminum core does not soften. To achieve these high temperatures the testbed includes an Air Torch system. The Air Torch is firing hot compressed air through a small hole of a high temperature resistance ceramic protecting the chip. To measure temperature Thermocouples were used.

In the case of the radiation experiments, the radiation source used was an electron beam obtained from a dynamitron accelerator. The electrons are accelerated at an energy of 1 MeV in a small vacuum chamber with a beam of 8". The fluxes in the small chamber was $4.E9 [e/(s.cm^2)]$ which is around 300 rad/sec. Figure 2 illustrates the incremental radiation profile to which the chips

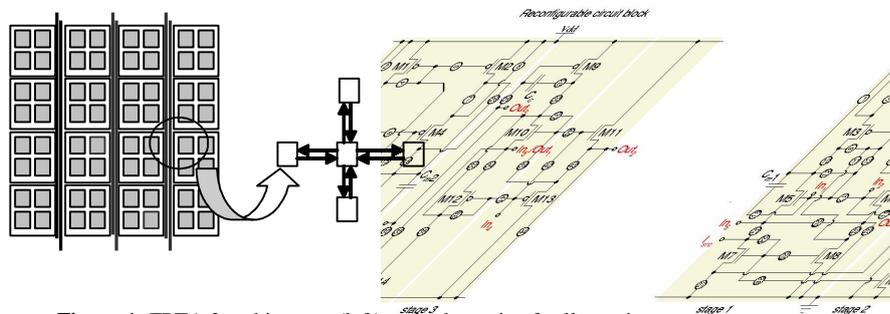


Figure 1: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

were subjected to over a period of 7 days.

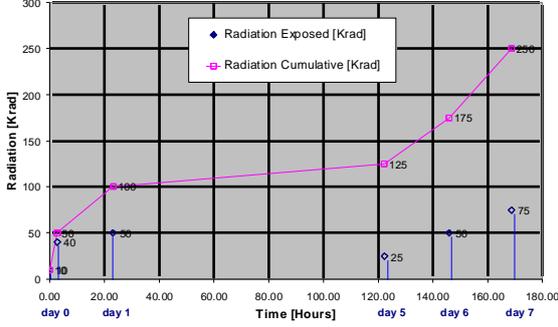


Figure 2: Cumulative radiation and experimental schedule.

4. Results

We describe here experiments for evolutionary recovery of the functionality of the following circuits: Halfwave Rectifier at 280°C; Low Pass Filter at 230°C; and Halfwave rectifier at 175kRads.

4.1 Half wave rectifier on FPTA-2 at 280°C

The objective of this experiment is to recover functionality of a half wave rectifier for a 2kHz sine wave of amplitude 2V using only two cells of the FPTA-2 at 280°C. The fitness function given below does a simple sum of error between the target function and the output from the FPTA.

The input was a 2kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for } (t_s < n/2) \\ R(t_s) - V_{\max}/2 & \text{otherwise} \end{cases} \quad (1)$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{\max} is 2V (the supply voltage). The output must follow the input during half-cycle, staying constant at a level of half way between the rails (1V) in the other half.

After the evaluation of 100 individuals, they were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), either among themselves or with an individual

from the elite, and then mutation (4% rate). The entire population was then reevaluated. Only two cells of the FPTA were allocated and used in this experiment.

Figure 3 depicts the response of the evolved circuit at room temperature and the degraded response at high temperature. Figure 4 shows the response of circuit obtained by running evolution at 280°C, where we can see that the functionality is recovered.

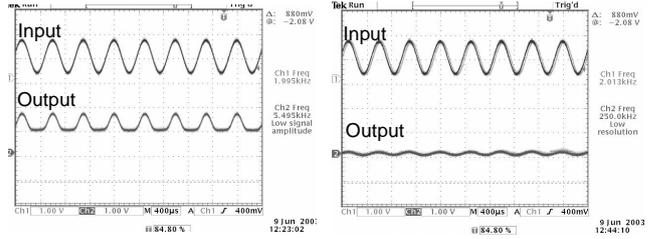


Figure 3: Input and output waves of the half-wave rectifier. On the left we show the response of the circuit evolved at 27°C. On the right we show the degraded response of the same circuit when the temperature is increased to 280°C.

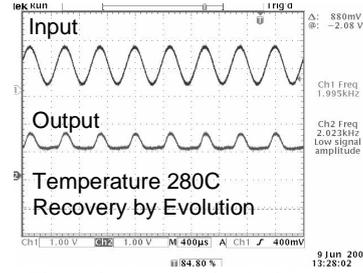


Figure 4: The solution for the Halfwave rectifier at 280°C.

4.2 Low-Pass Filter on FPTA-2 at 230°C

The objective of this experiment is to recover the functionality of a low-pass filter given ten cells of the FPTA-2. The fitness function given below performs a sum of error between the target function and the output from the FPTA in the frequency domain.

$$F = \sum_{f_s=0}^{n-1} (R(f) - T(f)) \quad (2)$$

Given two tones at 1kHz and 10kHz, the objective is to have at the output only the lowest frequency tone (1kHz). This hardware evolved circuit demonstrated that the FPTA-2 is able to recover active filters with some gain at 230°C.

Figure 5 shows the response of the evolved filter at room temperature and degradation at 230°C. Figure 6 shows the time response of the recovered circuit evolved at 230°C.

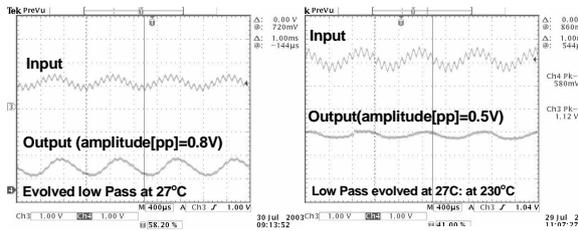


Figure 5: Low-Pass Filter. The graph displays the input and output signals in the time domain when the FPTA-2 was submitted to room temperature (left) and temperature of 230°C (right).

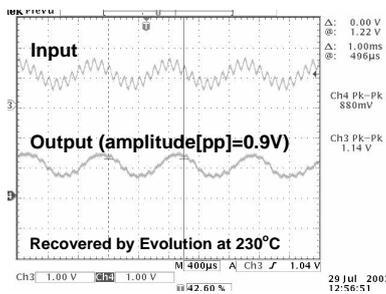


Figure 6: Recovered Low Pass Filter at 230°C.

At room temperature, the originally evolved circuit provides a gain of 3dB at 1kHz and a roll-off of -14dB/dec. When the temperature is increased to 230°C, the roll-off goes to -4dB/dec and the gain at 1kHz falls to -12dB. In the recovered circuit at high temperature the gain at 1kHz increases back to 1dB and the roll-off goes to -7dB/dec. Therefore the evolved solution at high temperature is able to restore the gain and to partially restore the roll-off.

4.3 Half Wave Rectifier at 175krads

This section describes the recovery of a half wave rectifier after the FPTA-2 is submitted to radiation. Figure 7(a) illustrates the response of a previously evolved rectifier after the chip is exposed to a radiation dose of 50krad. It can be observed that the circuit response is not affected by radiation. After exposure to radiation of up to 175Krad the rectifier malfunctions as the output response is identical to that of the input shown on Figure 7(b). When the evolutionary mechanism is activated, the correct output response is retained as shown in Figure 7(c).

5. Conclusions

The paper has presented a mechanism for adapting a mixed analogue reconfigurable platform for high temperature and radiation induced faults. Different experiments were carried out which exercised the reconfigurable device up to 280°C and 175Krad radiation dosages demonstrating that the technique is able to recover functionality of blocks such as rectifiers and filters.

Acknowledgement

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6. References

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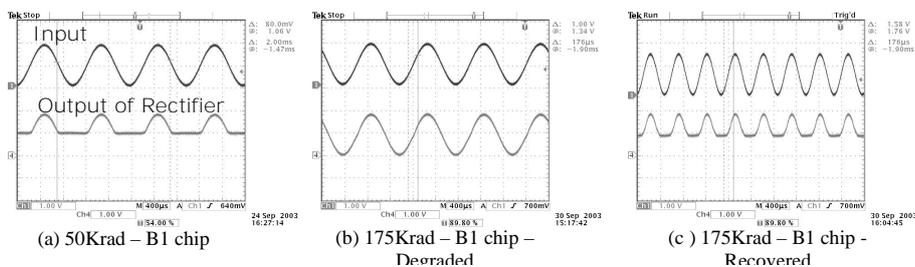


Figure 7: Response of the Rectifier circuit at (a) 50kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of rectification, followed by (c) recovery through Evolution.

