Analog circuit synthesis based on reuse of topological features of prototype circuits

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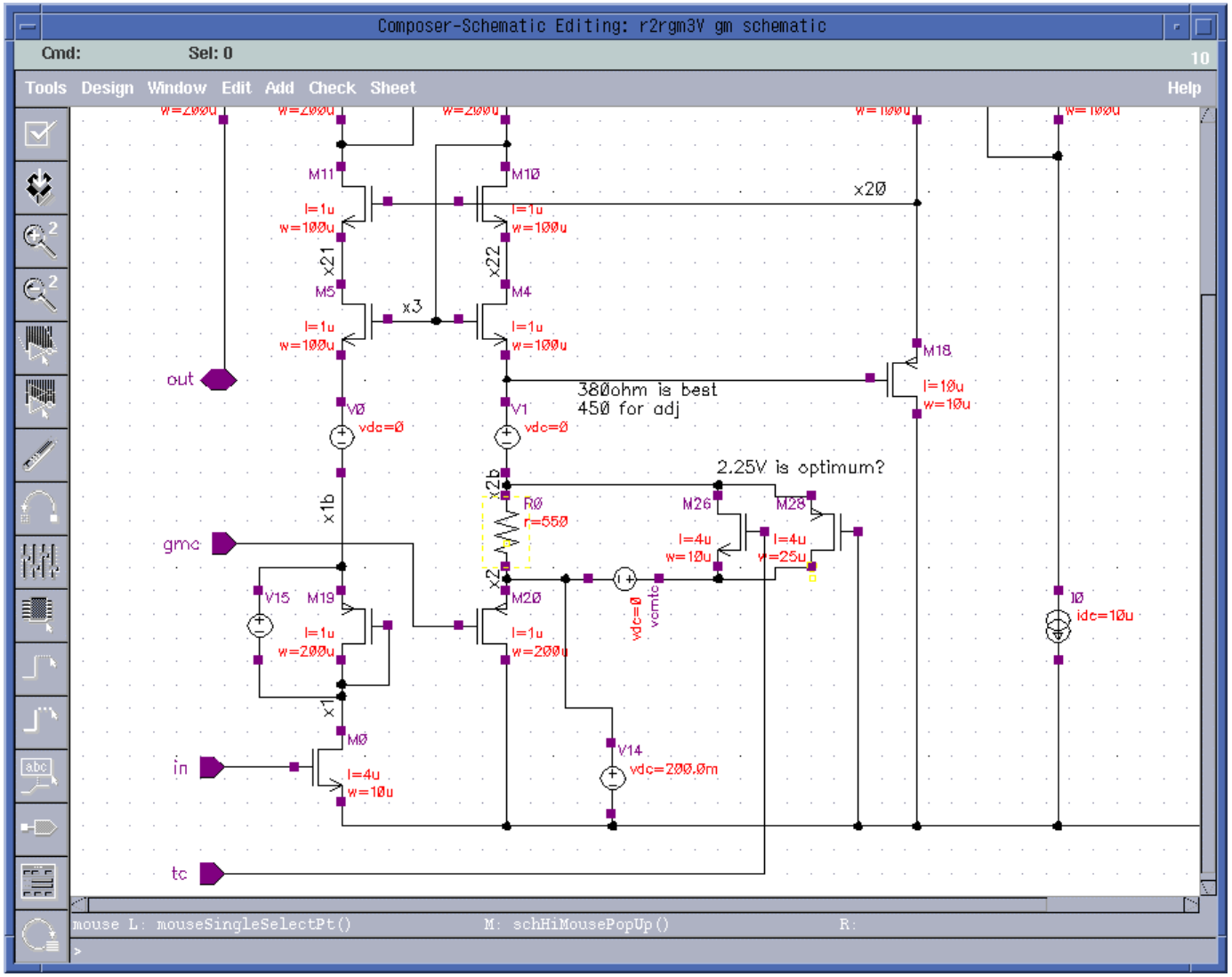
Outline

1. Background
2. Proposed method: 2-step synthesis
3. Application of genetic algorithm
4. Cubing circuit synthesis
5. Conclusions

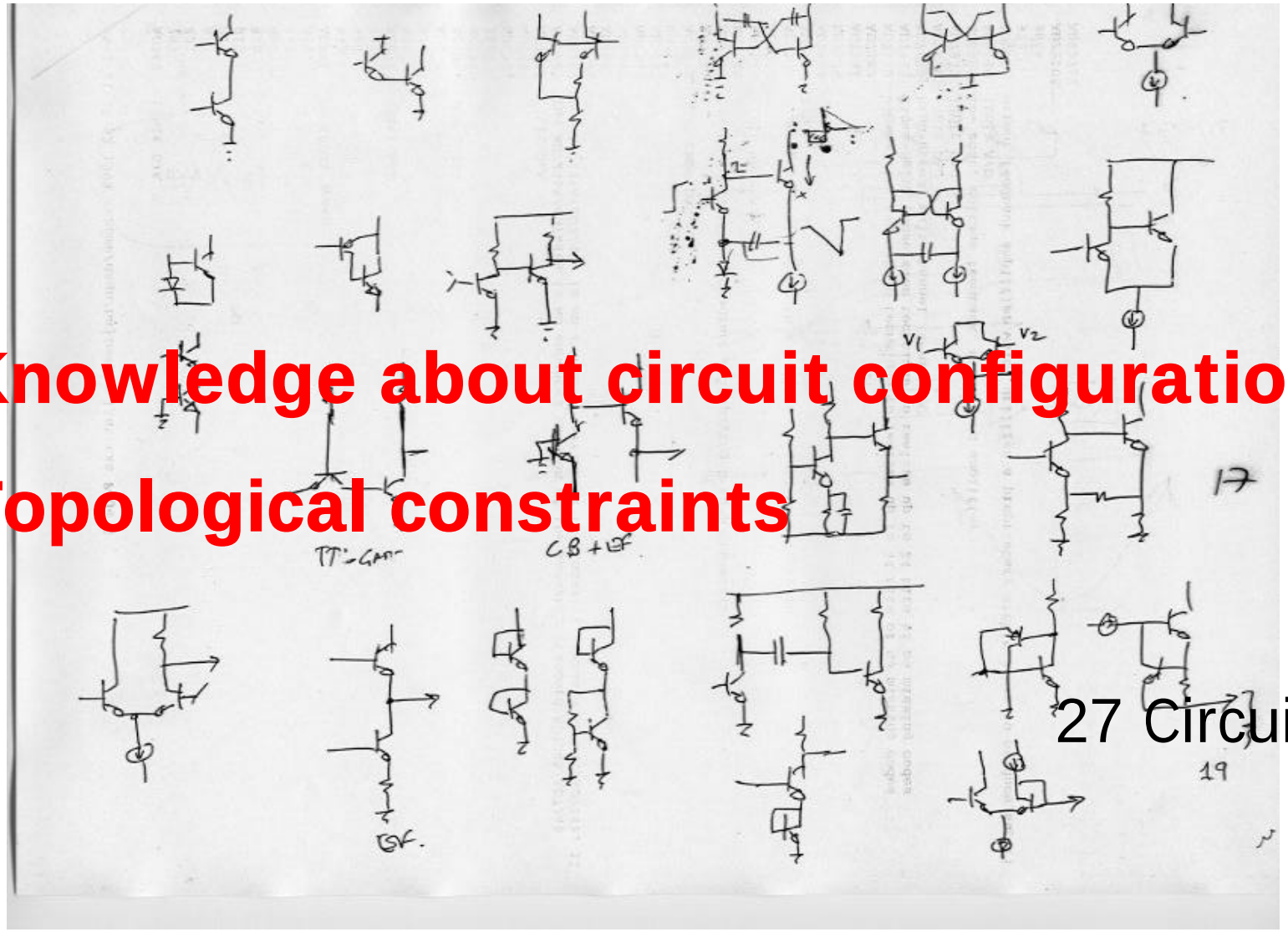
What is the analog circuit design?



Digital vs. Analog

	Digital	**Analog**
Circuit scale	Large	Small
Design methodology	HDL based	Schematic based
Design	Systematic	Intuitive
Synthesis System	Currently used	Not yet
Behavior of Transistors	Simple	Complex
Salary	High?	Higher??

Two-transistor circuits



Knowledge about circuit configurations

Topological constraints

27 Circuits

What are needed?

Basic building block have been developed

↓

Don’t need whole new circuit

But need some variation

↓

Reuse parts of circuit topologies

Analog Circuit Synthesis

- **Component Level Synthesis**
  - Difficulties on implementations on a real chip
  - Difficulties on reuse of human-designed circuits

- **Traditional Sub-circuit Level Synthesis**
  - Ex. Combinations of input stage and output stage of OPA's
  - Sub-circuits are designed by human

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Our target

- Online evolution

  Evolvable hardware (Analog FPGA.

  - Suppression of process variation
  - Minimum hardware
- Offline evolution

  Circuit Design

  - Component values
  - Circuit structure
    - Robustness
    - Automated design

Automated design of analog circuits

Proposed method

Reuse & Topological constrains

Prototype circuits

- Difficulties on reuse of human-designed circuits

  ? Learning from *prototype* circuits

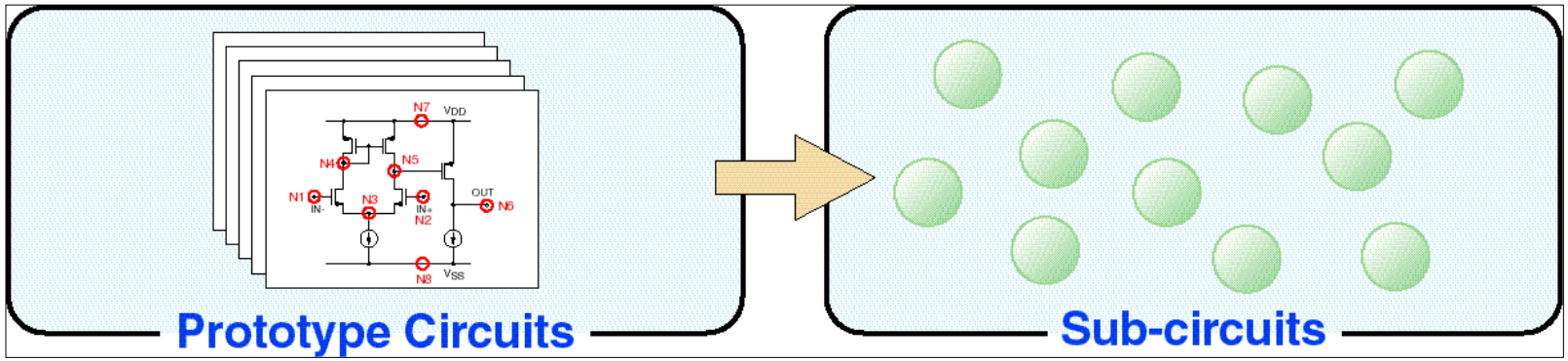
- Sub-circuits are designed by human

  ? Automatic decomposition of *prototype* circuits

2-step synthesis

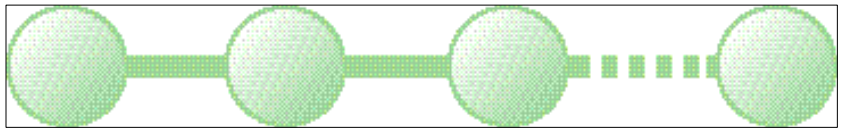
1st step: Learning step

Automatic Decomposition of Prototype circuit



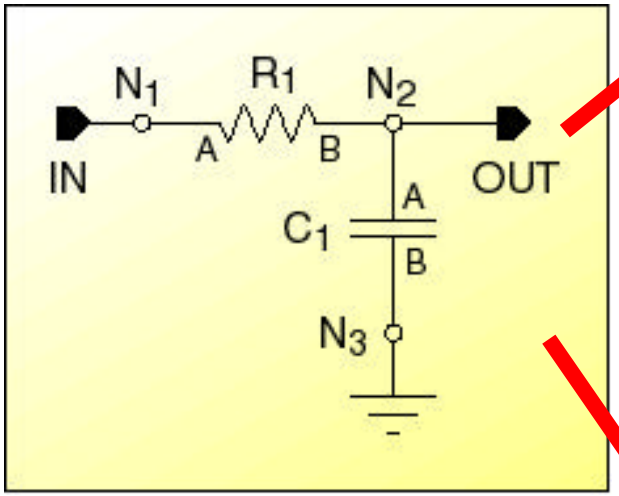
2nd step: Reuse step

Search the optimum combination of the sub-circuits

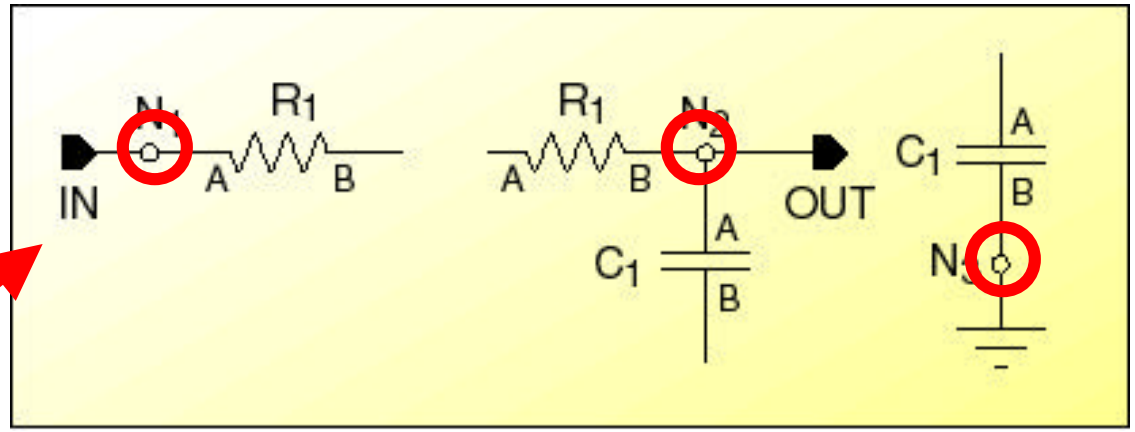


1st Step: Circuit Decomposition

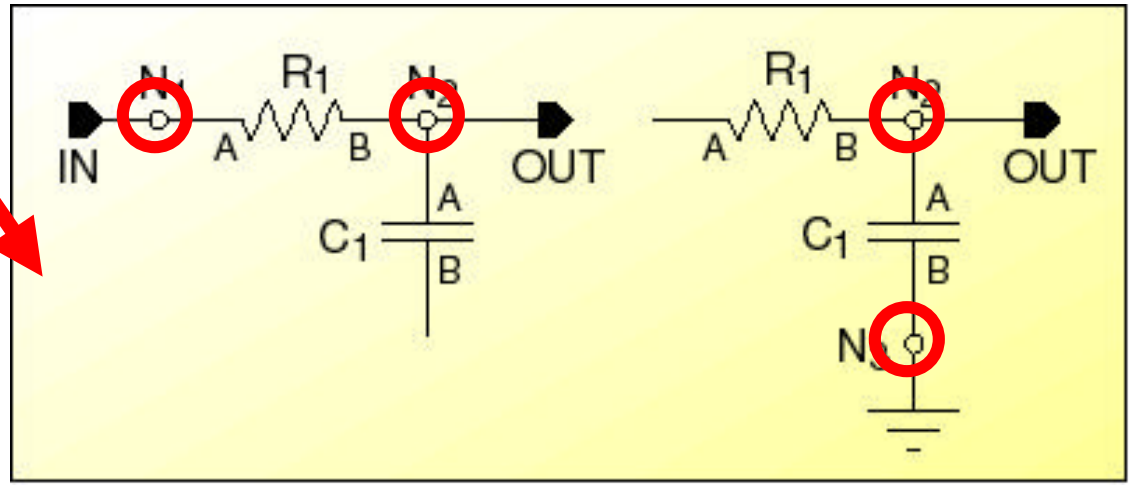
Prototype Circuit



1-node Sub-circuits



2-node Sub-circuits



2nd Step: Circuit Synthesis Scheme

Circuit ⟵ List of sub-circuits

$$C = T(\cdots(C_1 * C_2) * C_3) * \cdots) * C_l)$$

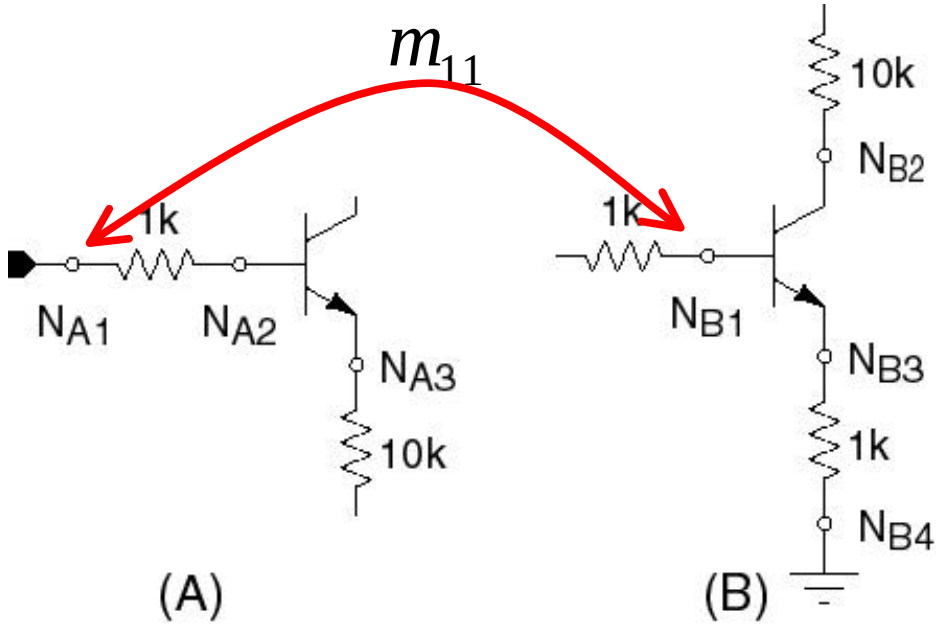
C : Abstracted circuit

C_i : Sub-circuit

$*$: Superimposing operator

T : Extraction operator

*: Superimposing #1



$$\mathbf{M} = \begin{pmatrix} m_{11} & m_{12} & m_{13} & m_{14} \\ m_{21} & m_{22} & m_{23} & m_{24} \\ m_{31} & m_{32} & m_{33} & m_{34} \end{pmatrix} = \begin{pmatrix} 0.5 & 0.4 & 0.5 & 0.5 \\ 1.0 & 0.4 & 0.5 & 0.5 \\ 0.4 & 0.5 & 0.9 & 0.5 \end{pmatrix}$$

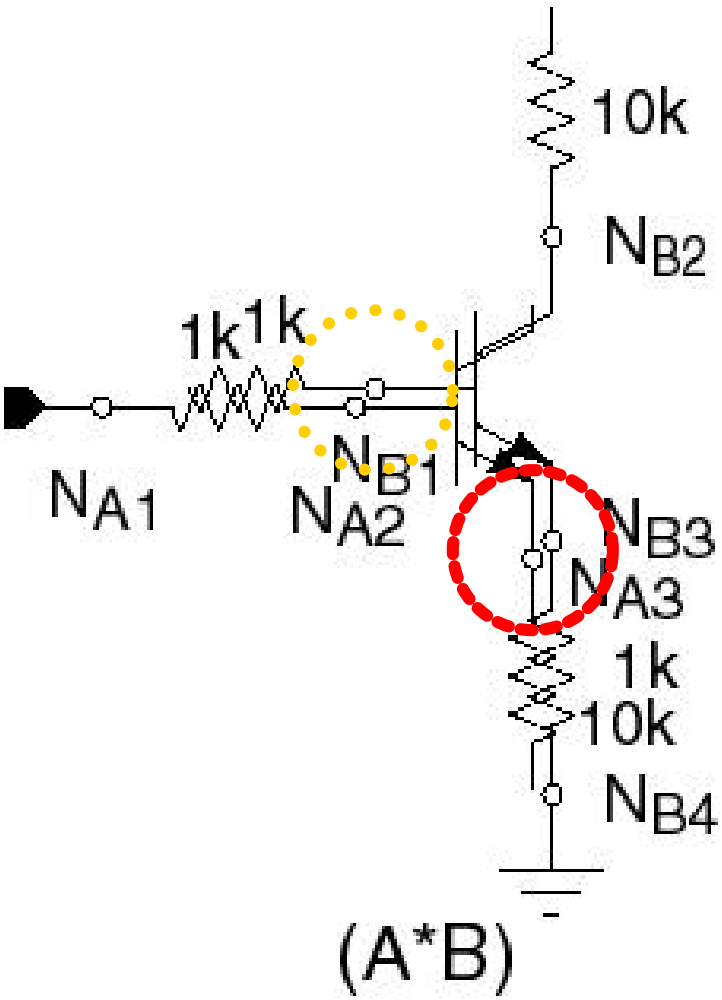
$$m_{11} = \frac{2T_C}{T_{A1} + T_{B1}} - w_m \max\{0, L_i\} = \frac{2 \times 1}{2+2} - 0.2 \times 0 = 0.5$$

*: Superimposing #2

$$\mathbf{M} = \begin{pmatrix} m_{11} & m_{12} & m_{13} & m_{14} \\ m_{21} & m_{22} & m_{23} & m_{24} \\ m_{31} & m_{32} & m_{33} & m_{34} \end{pmatrix}$$

$$= \begin{pmatrix} 0.5 & 0.4 & 0.5 & 0.5 \\ 1.0 & 0.4 & 0.5 & 0.5 \\ 0.4 & 0.5 & 0.9 & 0.5 \end{pmatrix}$$

$$m_T = 0.7$$



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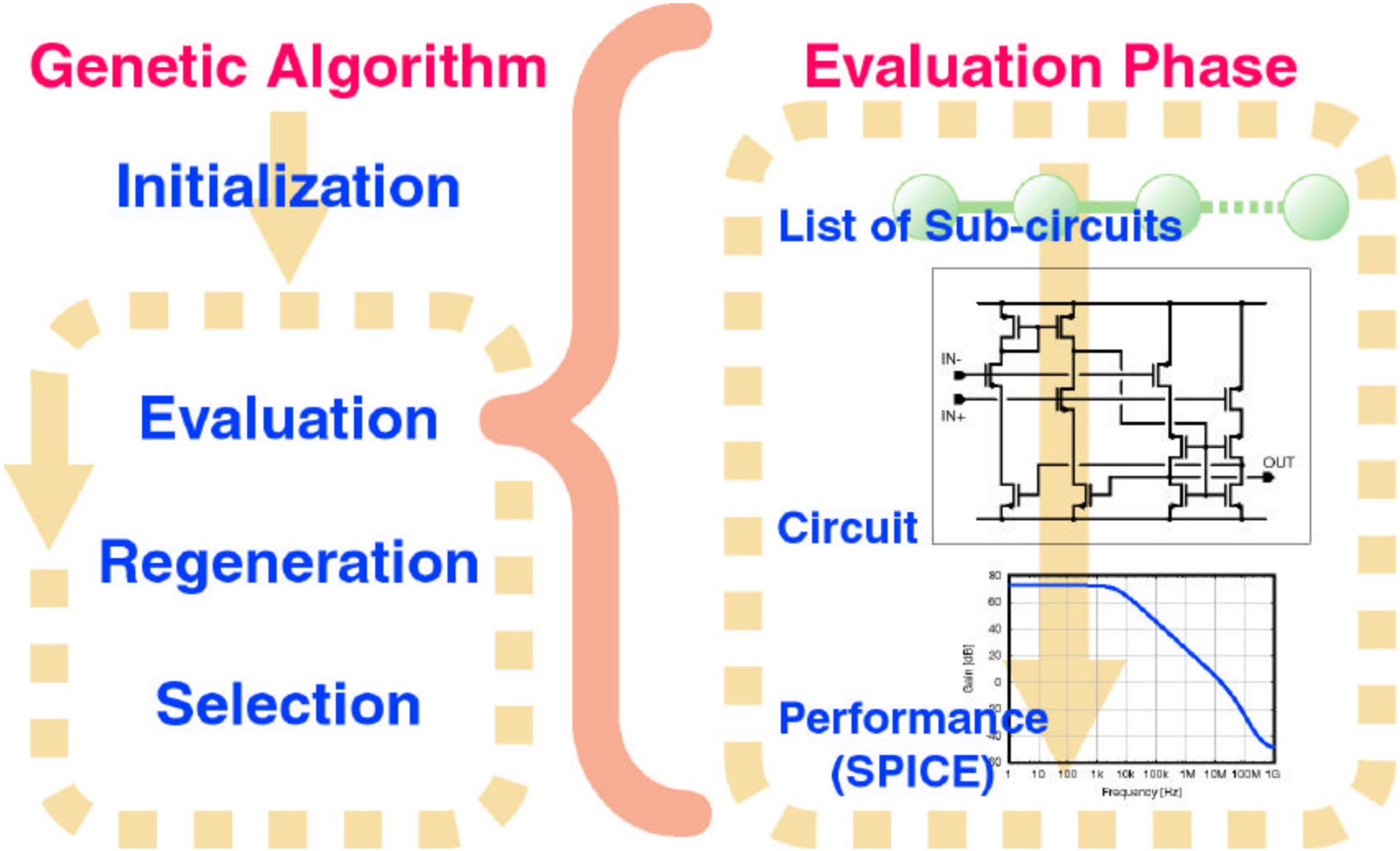
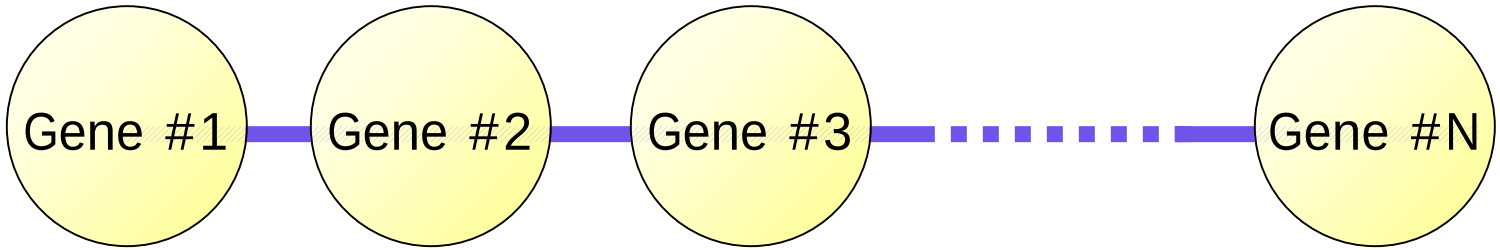
2nd Step: Optimization



Gene expression and operations



1. Crossover
2. Parameter mutation
3. Self crossover
4. Exchange a gene for a gene in gene pool
5. Inversion

Best circuit is decomposed and stored in gene pool

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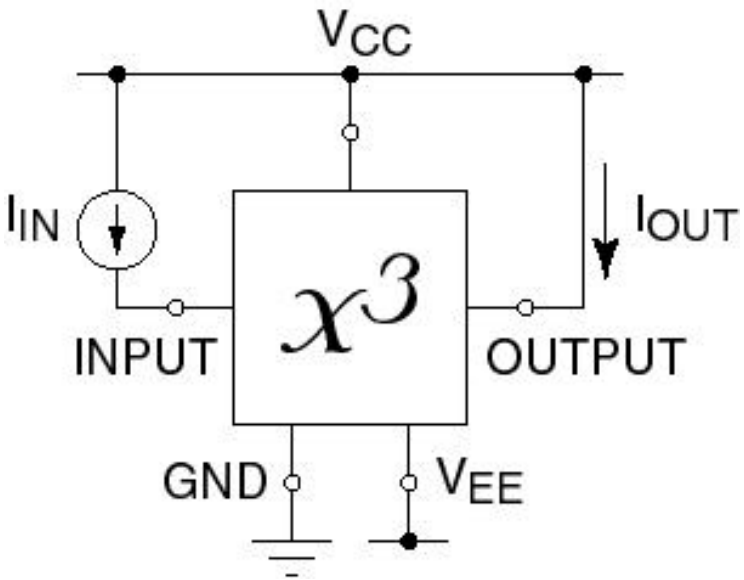
Cubing Circuit: Evaluation

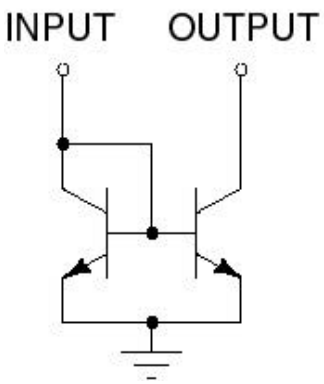
Definition

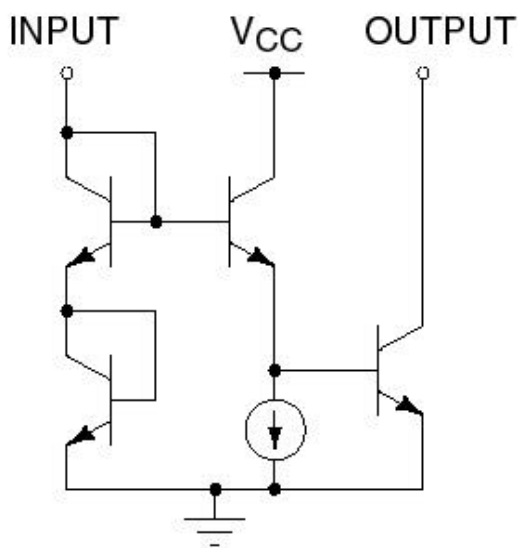
$$\frac{I_{OUT}}{I_0} = \left(\frac{I_{IN}}{I_0}\right)^3$$

Connection for Eval.

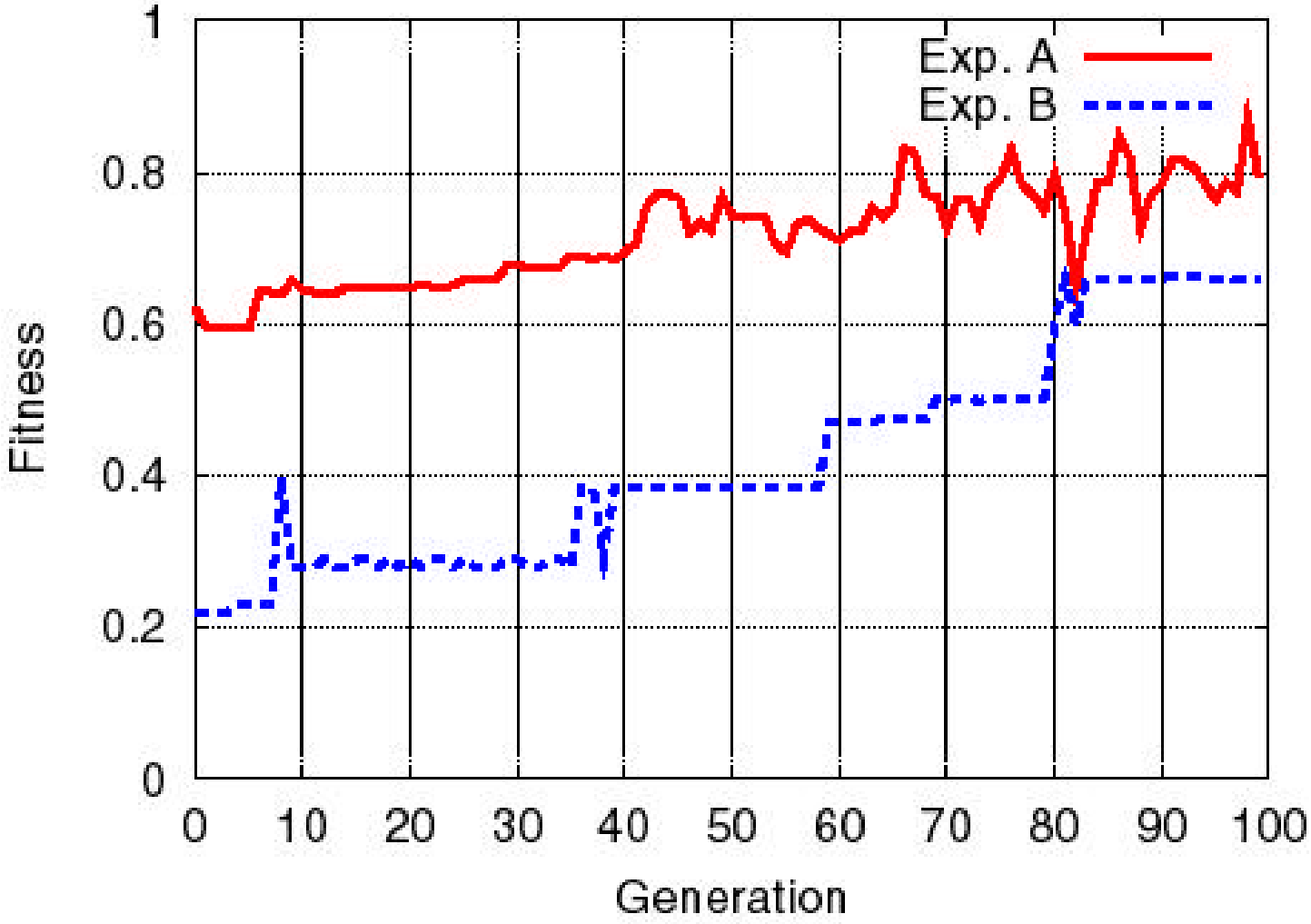


Prototype Circuits





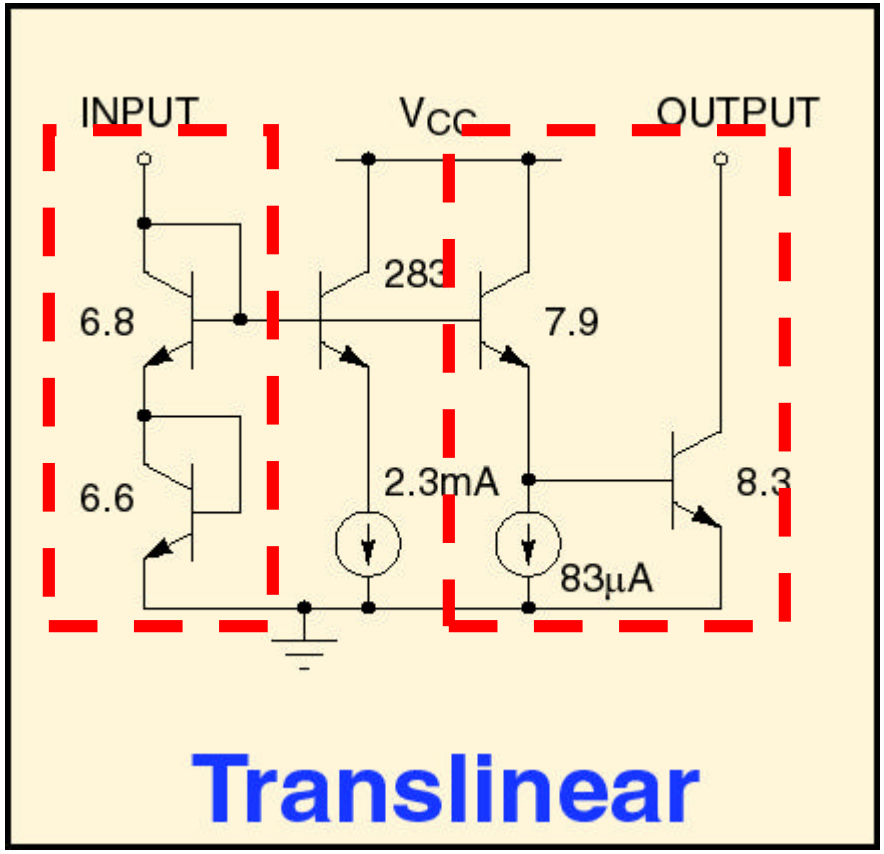
Cubing Circuit: Fitness Transition

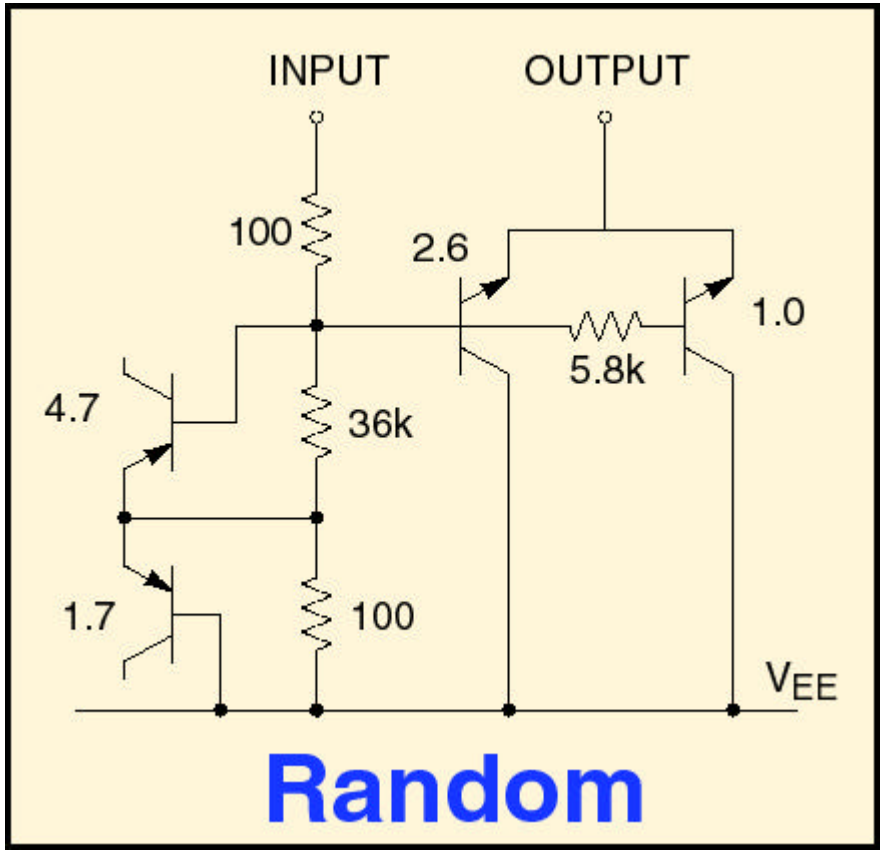


Cubing Circuit: Parameters

Minimum node size	1
Maximum node size	3
Minimum gene length	2
Maximum gene length	15
Population	500
Threshold of matching	0.6
Coeff. of multiple circuits	0.7
Coeff. of parameter	0.2

Cubing Circuit: Synthesized Circuits

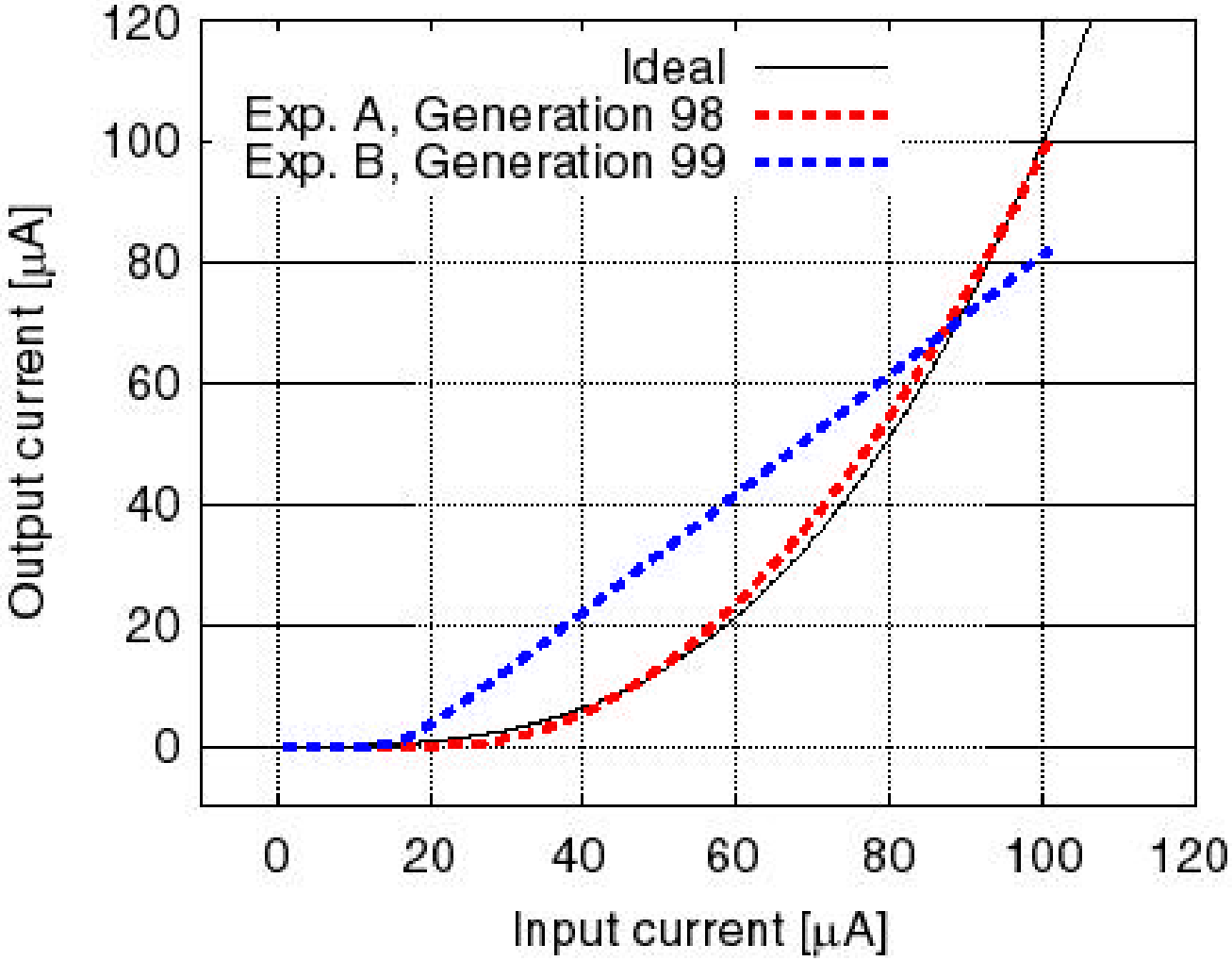




Exp. A

Exp. B

Cubing Circuits: Characteristics



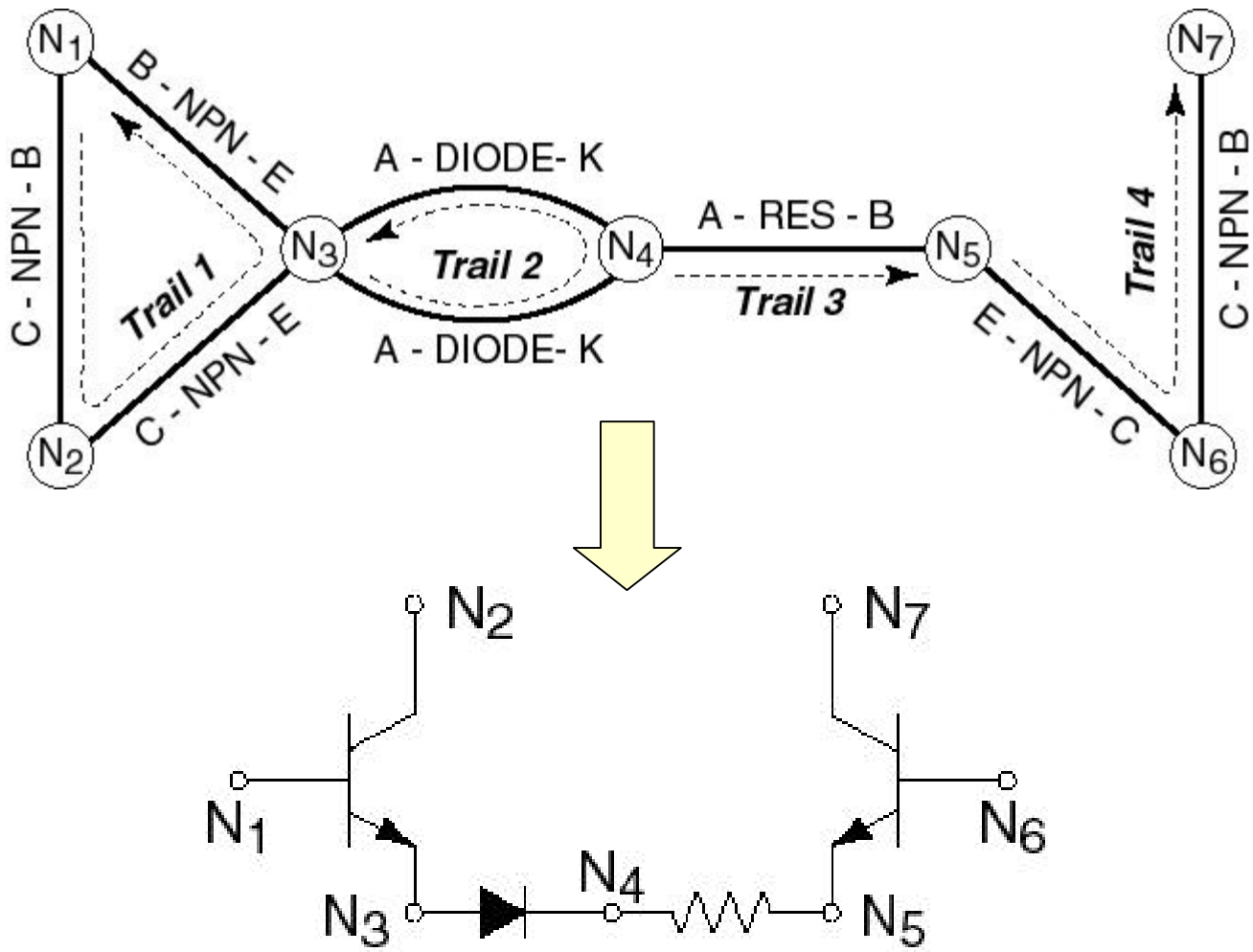
Conclusions

- 2-step synthesis composed of learning and reuse was proposed.
- Moderate constrains on configuration were introduced.

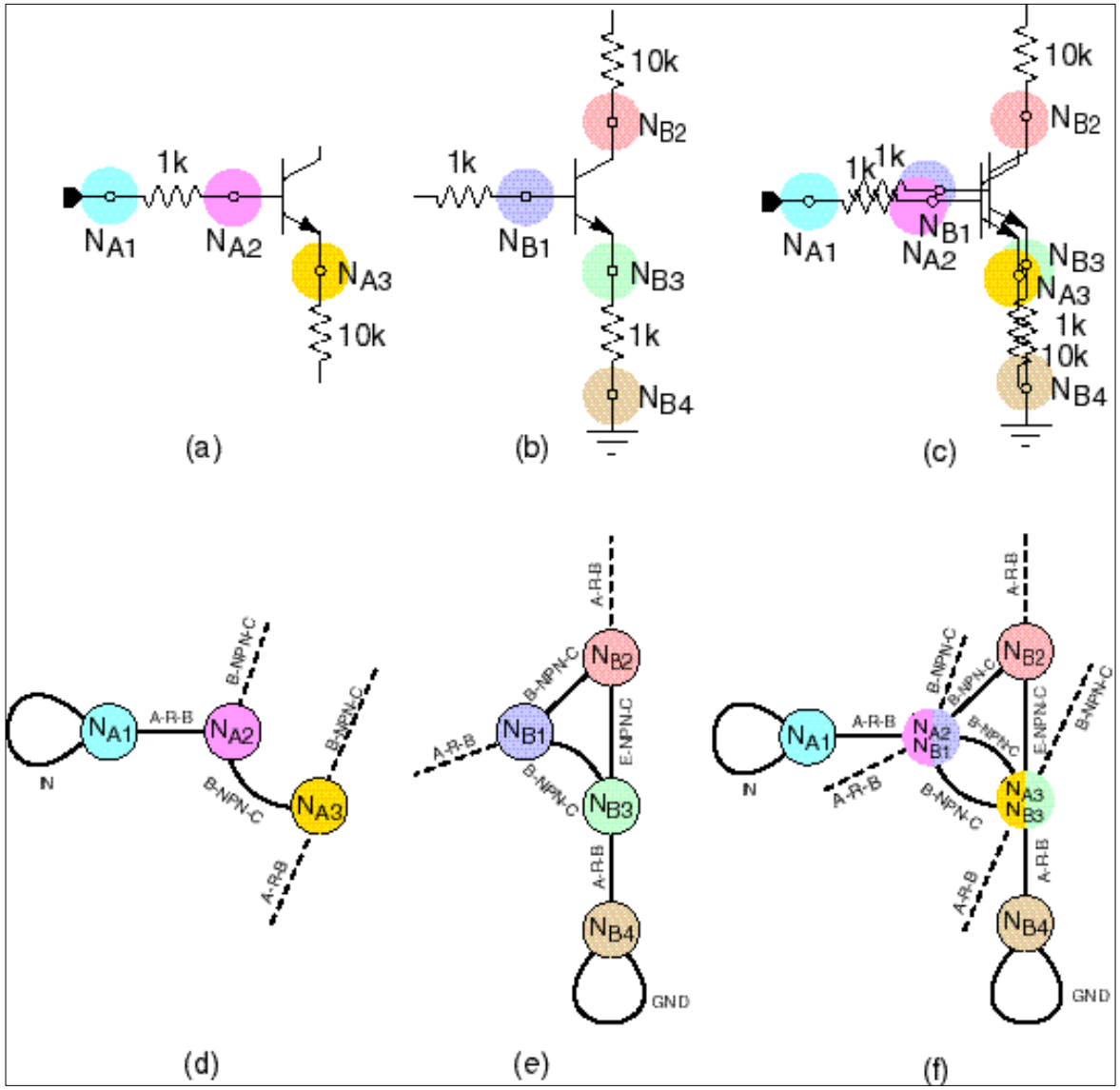
- Future works:
  - Applications on more complex circuits
  - Analysis of synthesis procedures

Thank you

T : Circuit Extraction



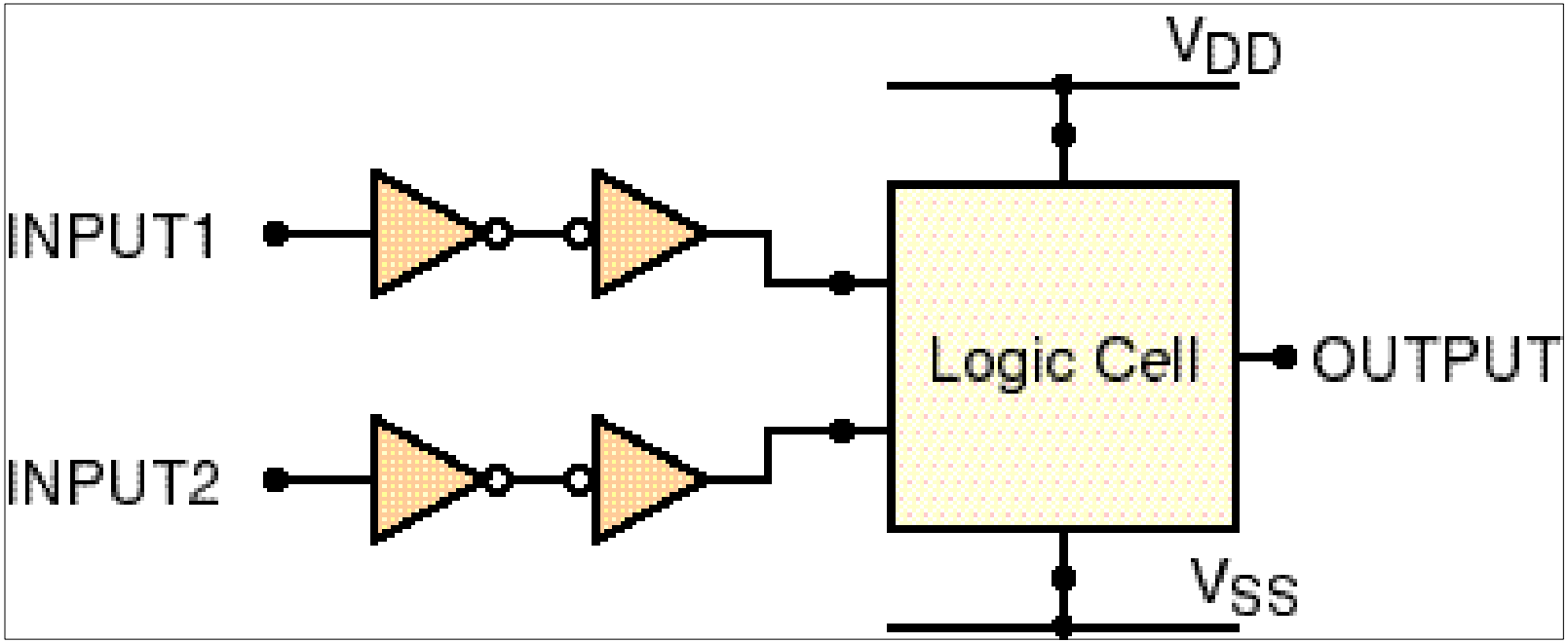
Graphic Representation



Outline

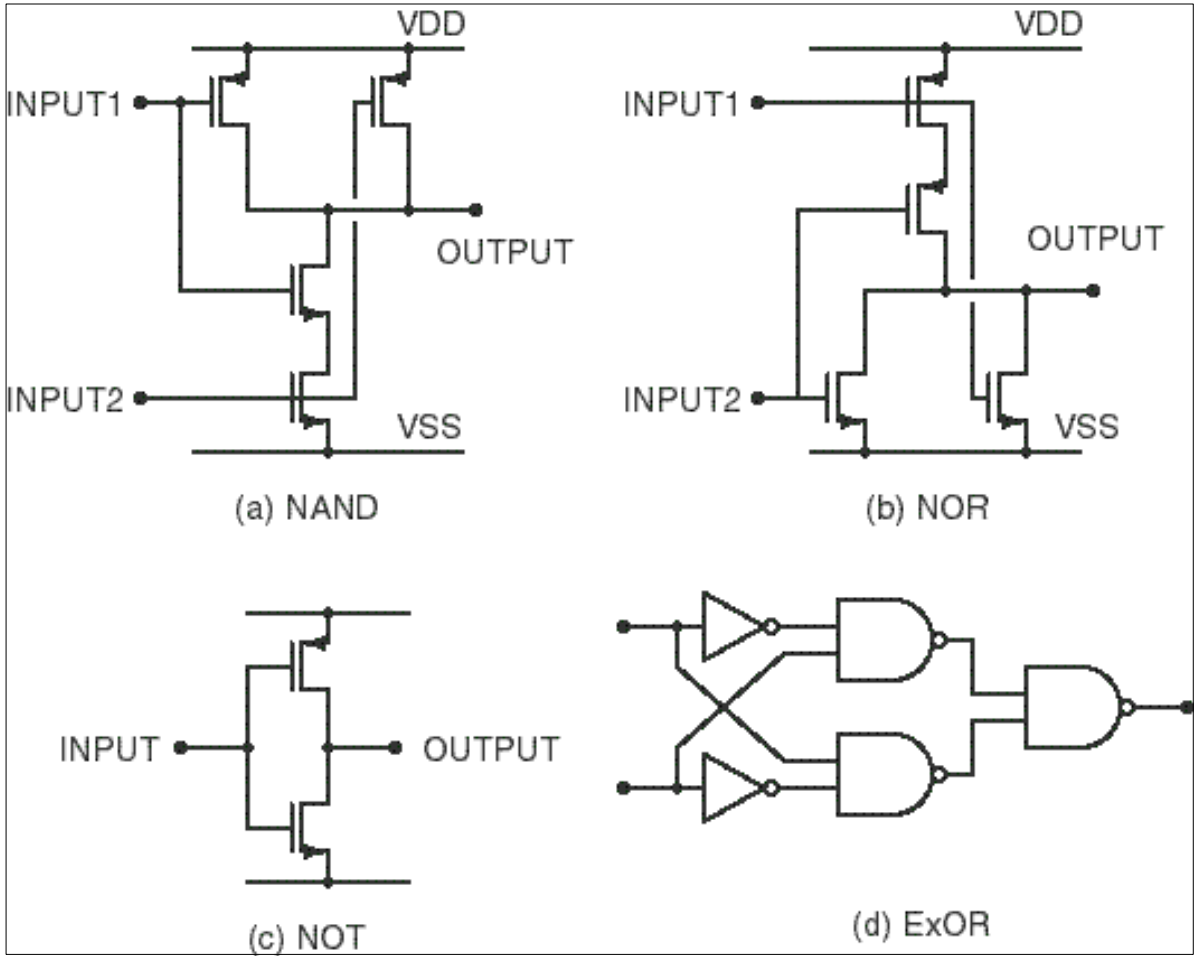
1. Background
2. Proposed method: 2-step synthesis
   1. English sentence synthesis
   2. Extraction and synthesis
3. Application of genetic algorithm
4. Cubing circuit synthesis
5. Logic gates synthesis
6. Conclusions

Logic Gates: Evaluation



- Low level threshold: 1V
- High level threshold: 4V

Logic Gates: Prototype Circuits



Reversed Inputs version is also used

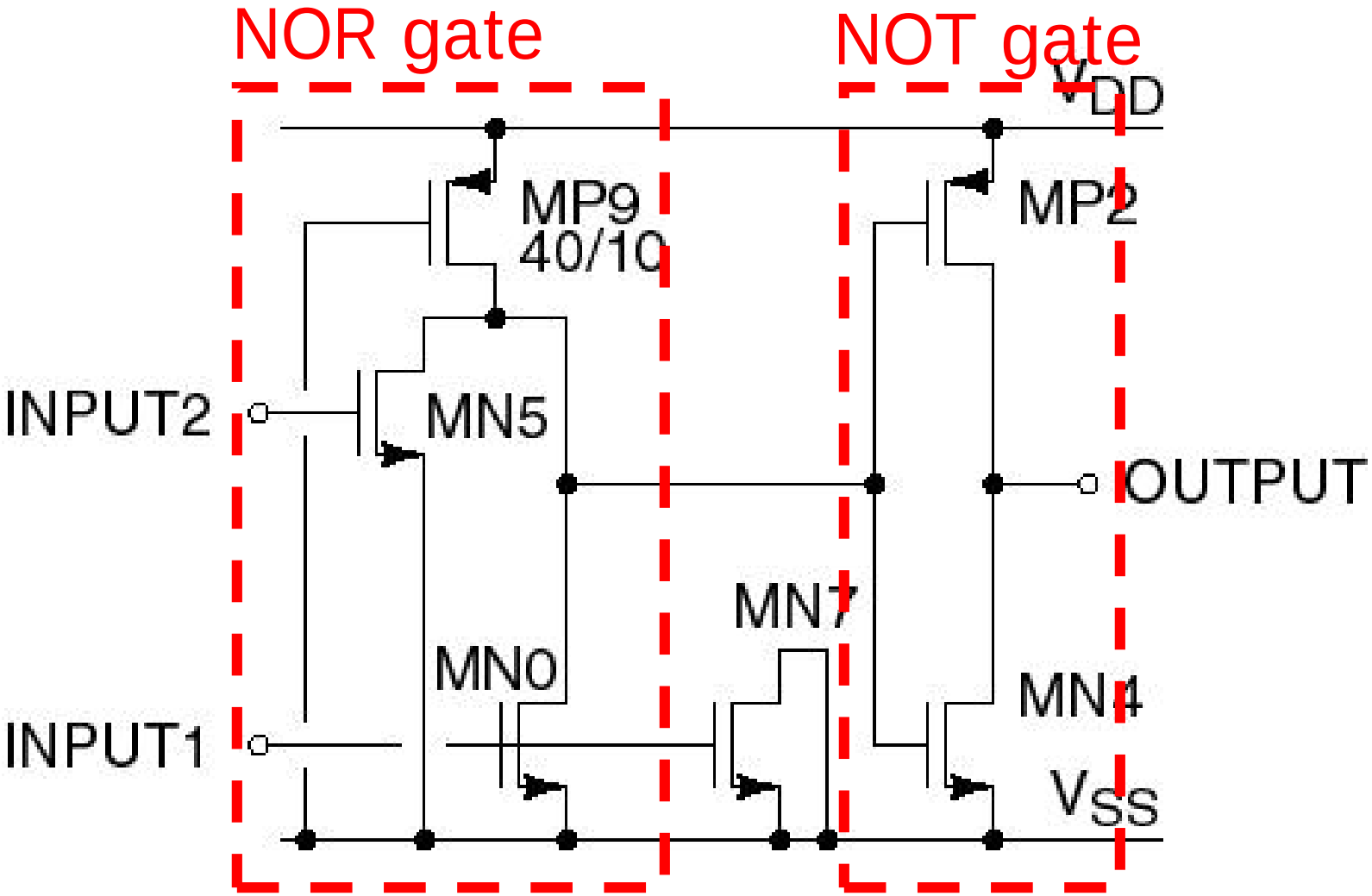
Logic Gates: Parameters

Minimum node size	1
Maximum node size	3
Minimum gene length	2
Maximum gene length	10
Population	1000
Threshold of matching	0.7
Coeff. of multiple circuits	0.2
Coeff. of parameter	0.1

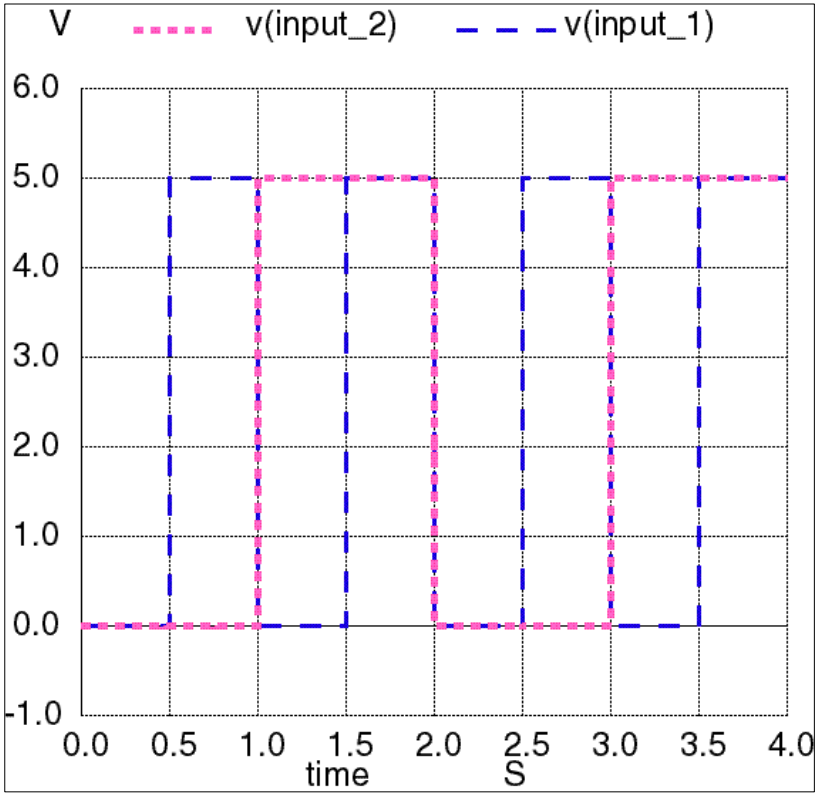
Logic Gates: Results

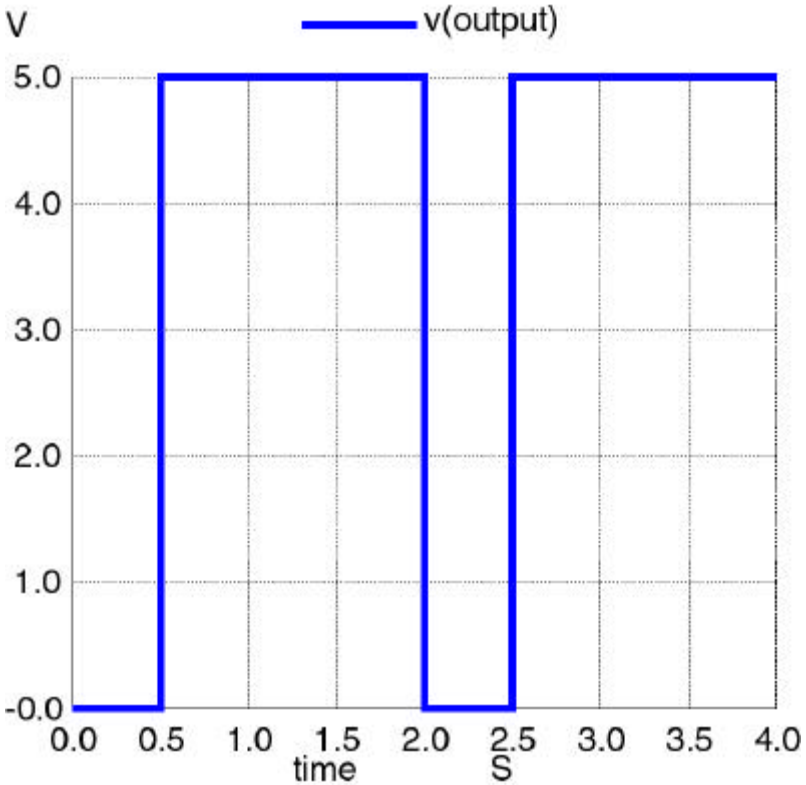
Gate	OUTPUT	Time [min]	Gen.	Gate	OUTPUT	Time [min]	Gen.
	0000	0	0	NOR	1000	1	0
AND	0001	19	6	/Ex-OR	1001	66	20
	0010	3	0		1010	0	0
	0011	0	0		1011	22	7
	0100	4	13		1100	0	0
	0101	1	0		1101	17	5
Ex-OR	0110	297	68	NAND	1110	6	2
OR	0111	2	0		1111	0	0

Logic: Synthesized OR gate

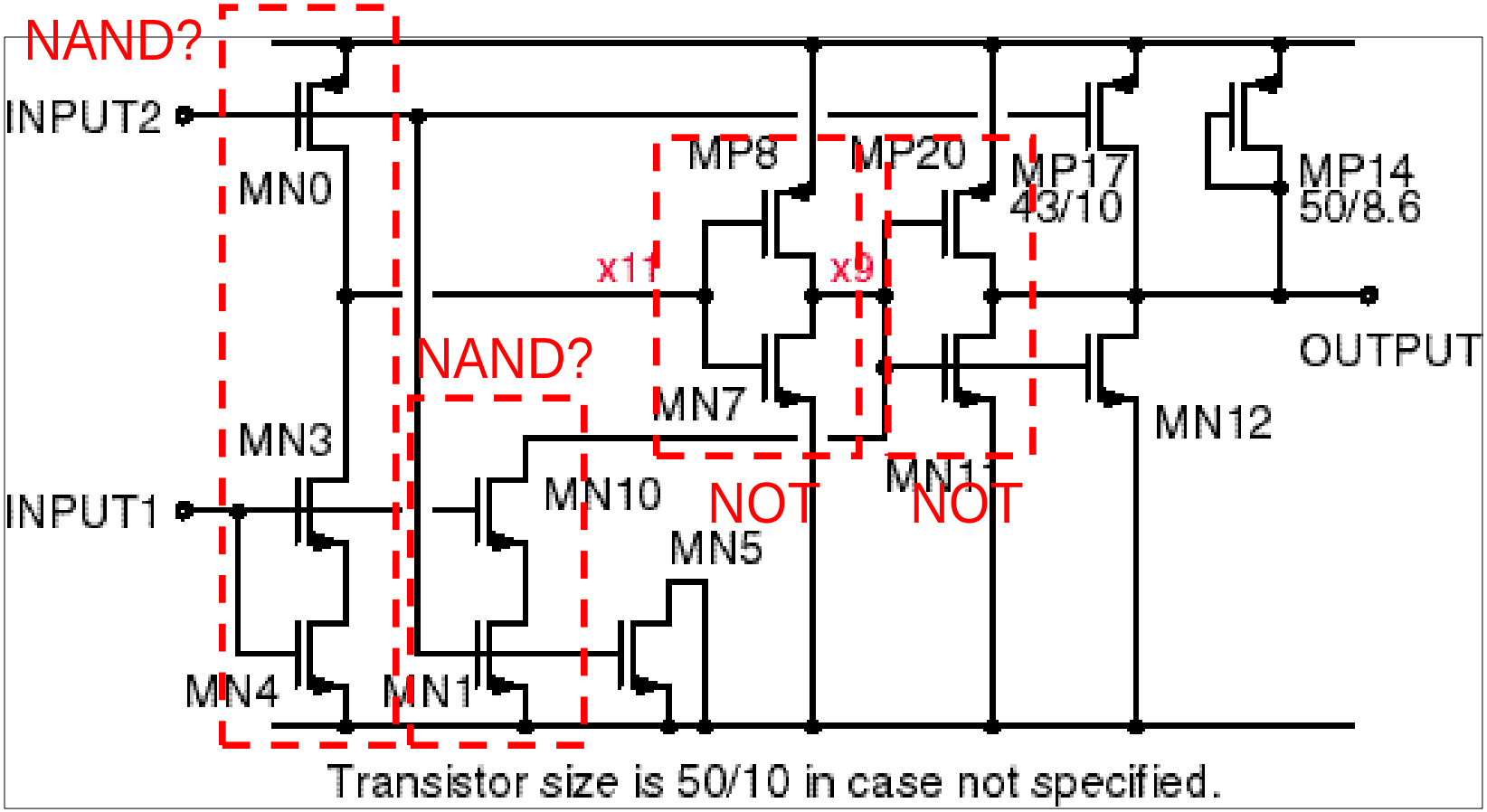


Logic: OR Waveform



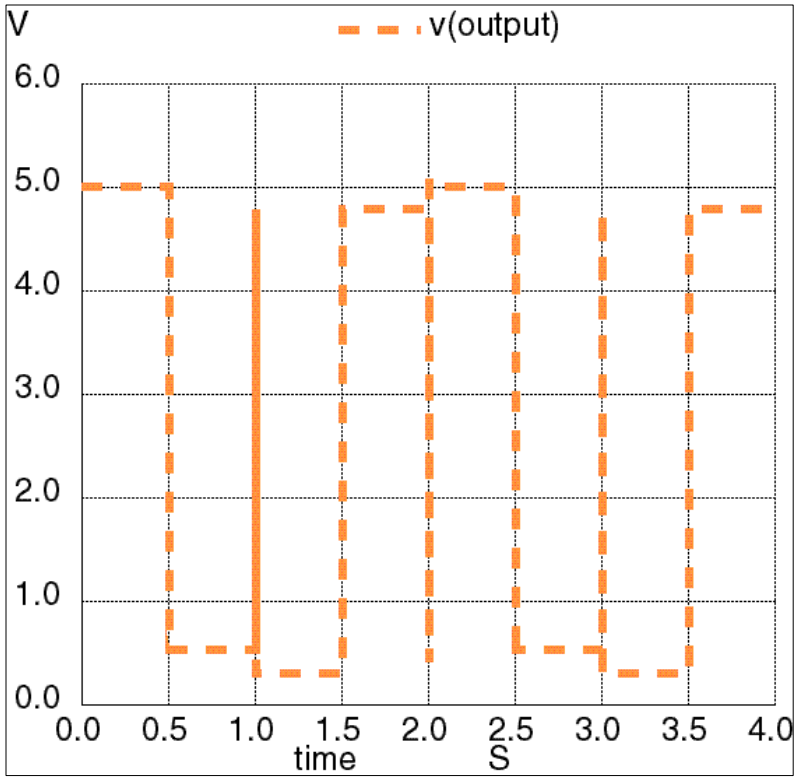


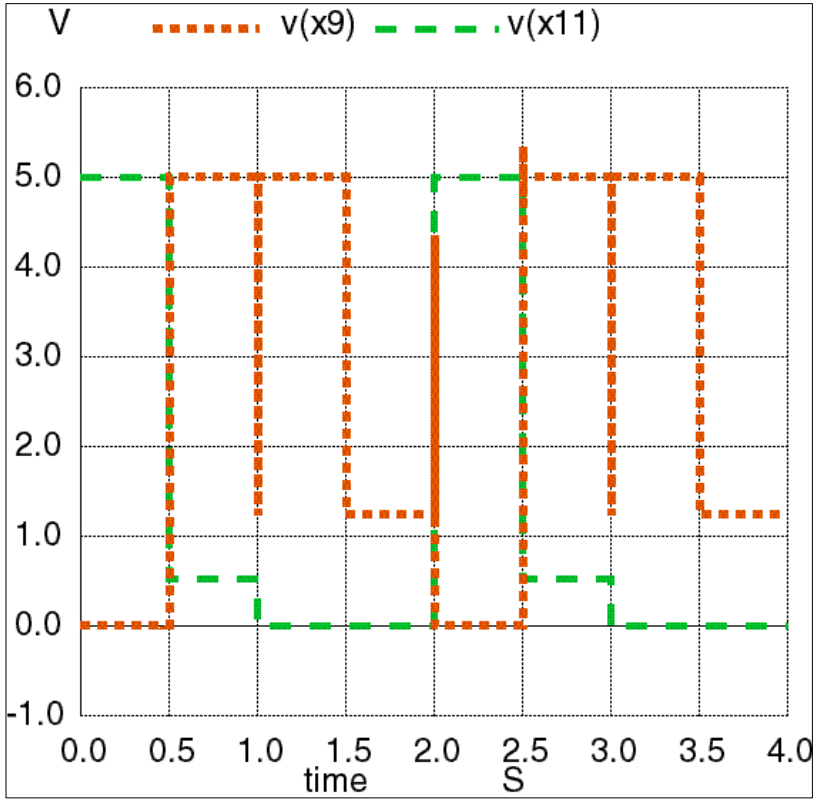
Logic: Synthesized Ex-OR gate



13 transistors (Prototype Ex-OR requires 16 transistors)

Logic: Ex-OR Waveform





Logic Gates: Conclusions

- All types of 2-IN 1-OUT type logic cell are synthesized.
- Synthesized circuits are based on prototype configurations.

- Meaningless connections exist.