New Genetic Operators to Facilitate Understanding of Evolved Transistor Circuits

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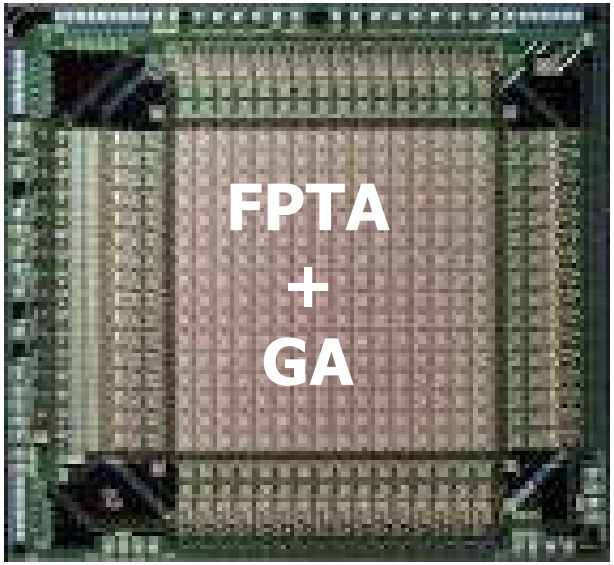
Evolvable Hardware Conference 2004

Overview

- Evolvable hardware system overview – the Heidelberg FPTA
- Introduction of new variation operators for our implementation of the GA
- Comparison to the straight forward implementation of the genetic operators in two experiments:
  - Comparators
  - Logic gates (AND, OR, XOR)
- Achievements using the new genetic operators:
  - Simulation of the evolved circuits outside the FPTA
  - Comparison of simulation and on-chip measurement
  - Improvement of the circuits

Facilitate Understanding of Evolved Circuits



- evolve valid circuits
- simulate evolved circuit outside the FPTA -> transferability
- minimize substrate dependency
- generate human understandable schematics

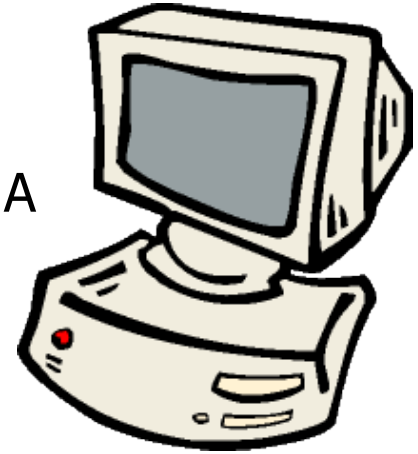
Innovation of all-purpose analog circuits

!?

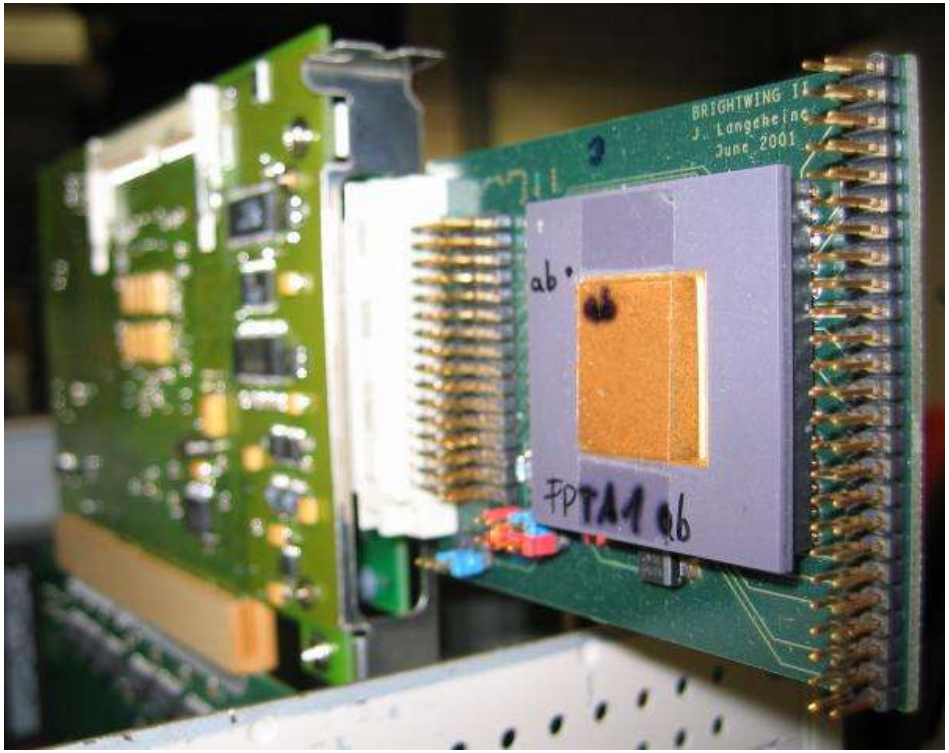
Next step:
- new genetic operators -> valid circuits
- extracting netlists -> simulation

Hardware Evolution System

- GA



- candidate circuit
  - testpattern
    - configuration data

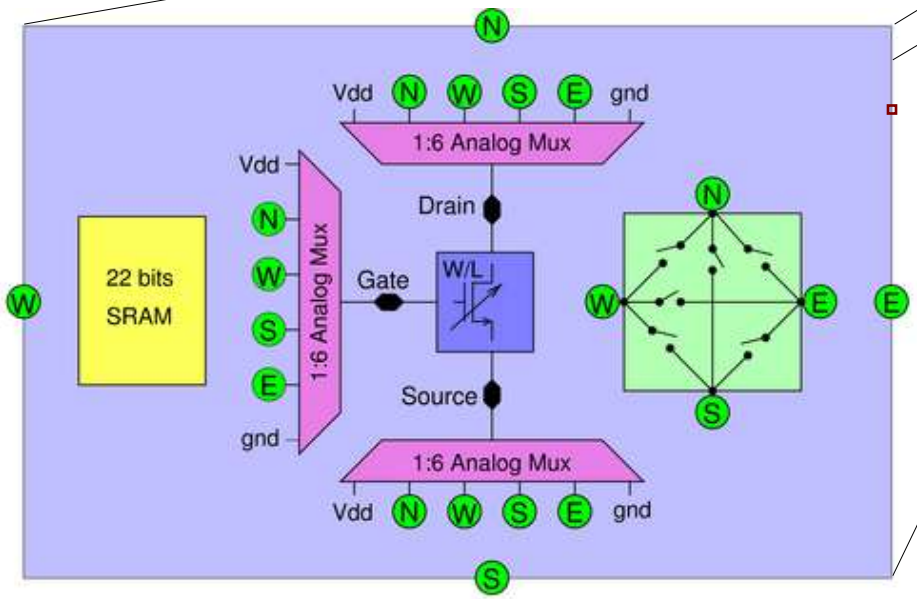


- measured data

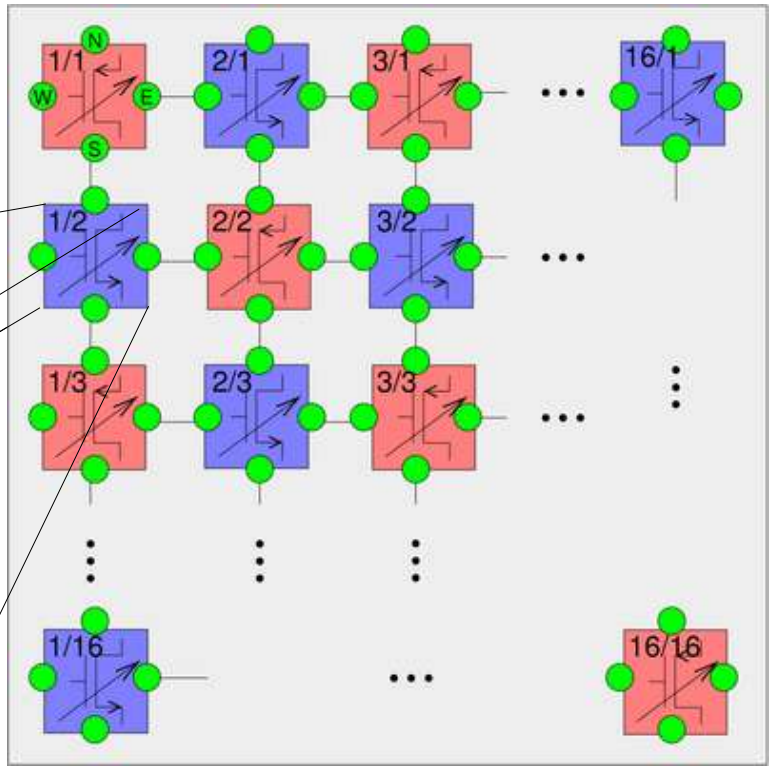
FPTA Transistor Array

Transistor configuration:

- adjustable W/L ratio
- terminals -> N,S,W,E, vdd or gnd



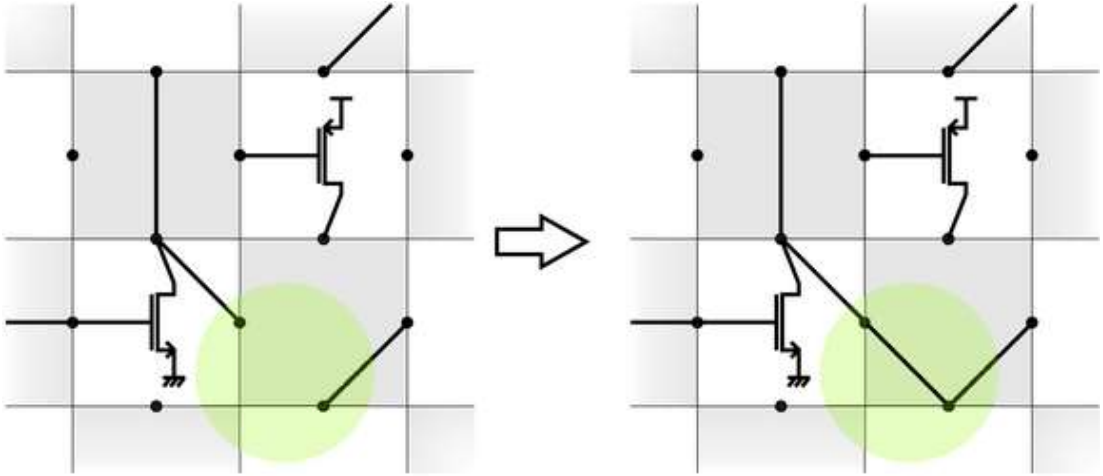
Note: All of the cardinal points N,W,S,E possess the same potential respectively



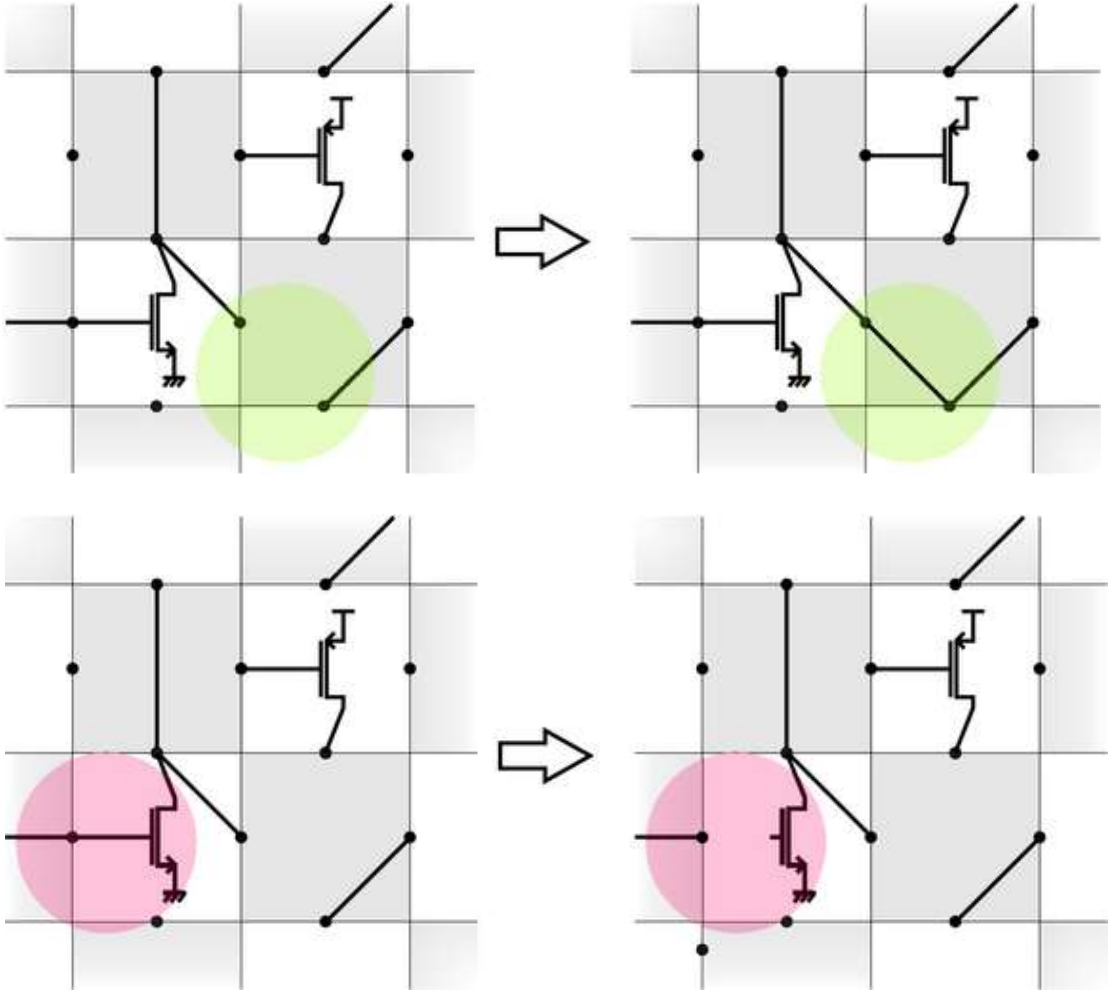
Routing capabilities:

- interconnect N,S,W,E

Basic GA : Mutation

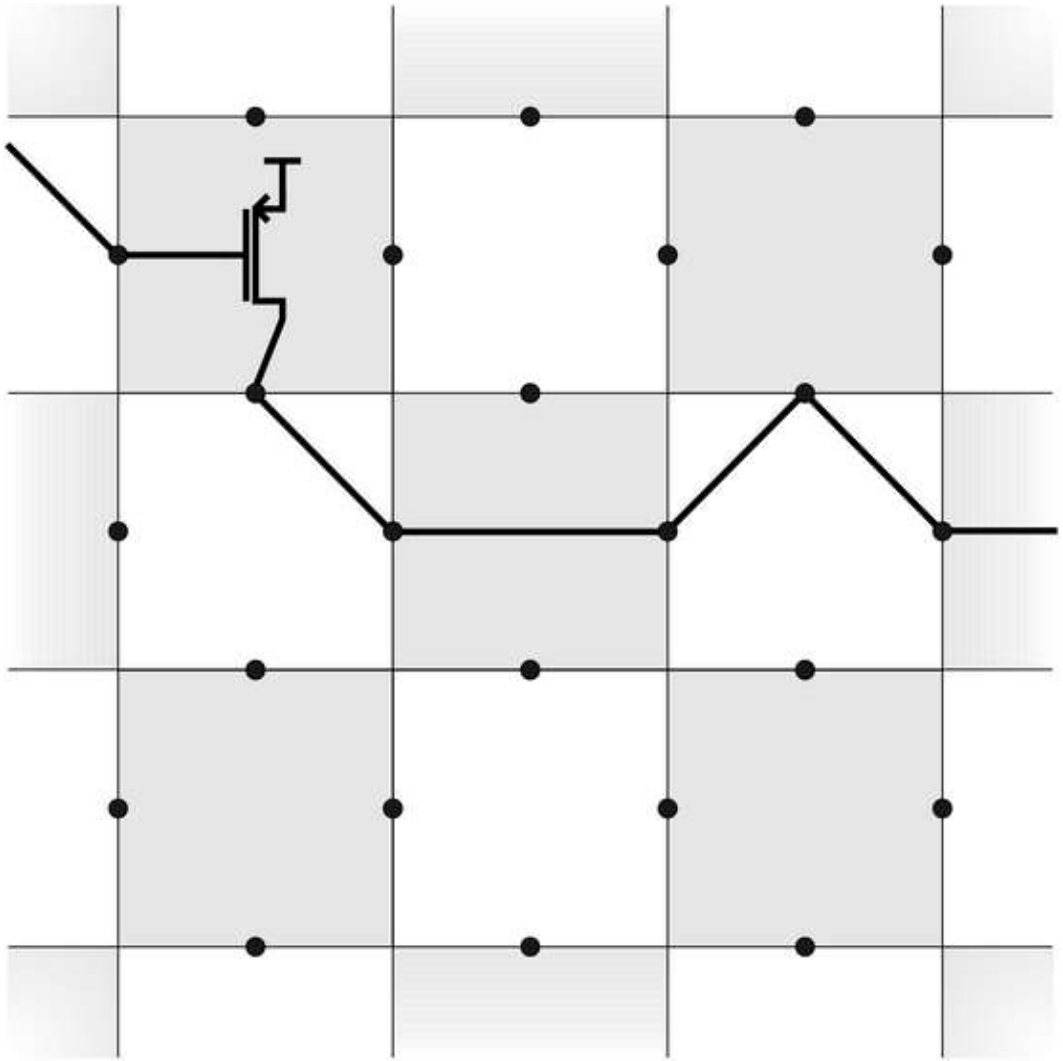


Basic GA : Mutation

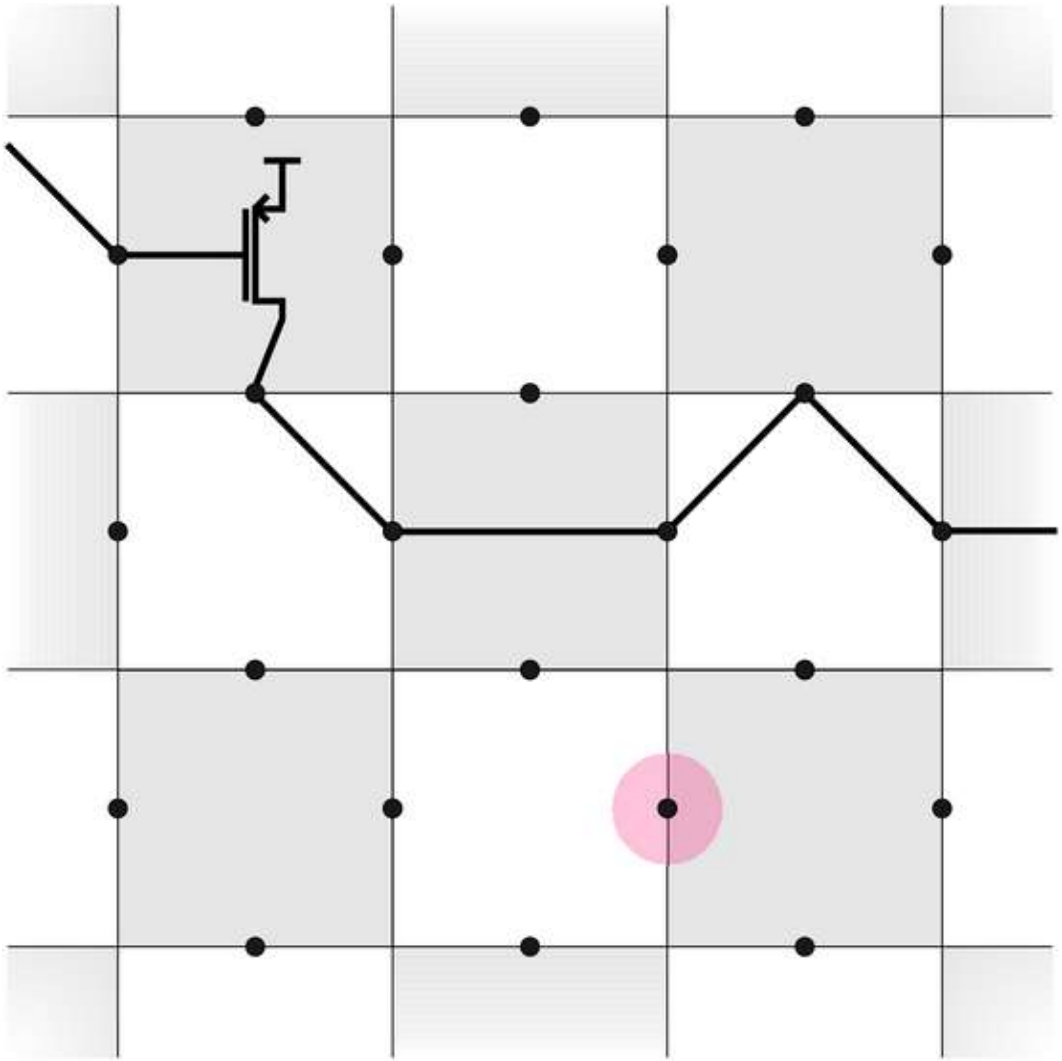


Problems:
- floating nodes
- no transfer

Turtle GA : Mutation

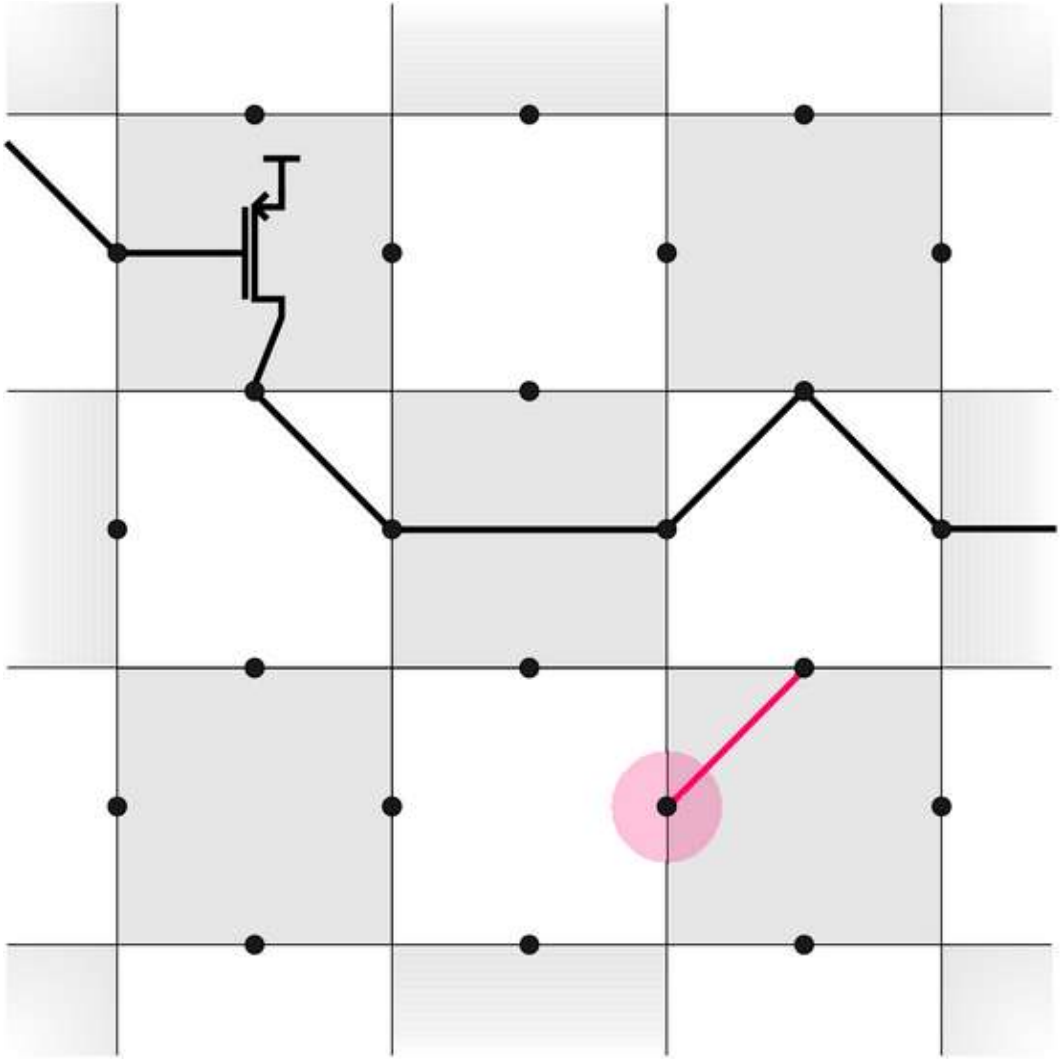


Turtle GA : Mutation



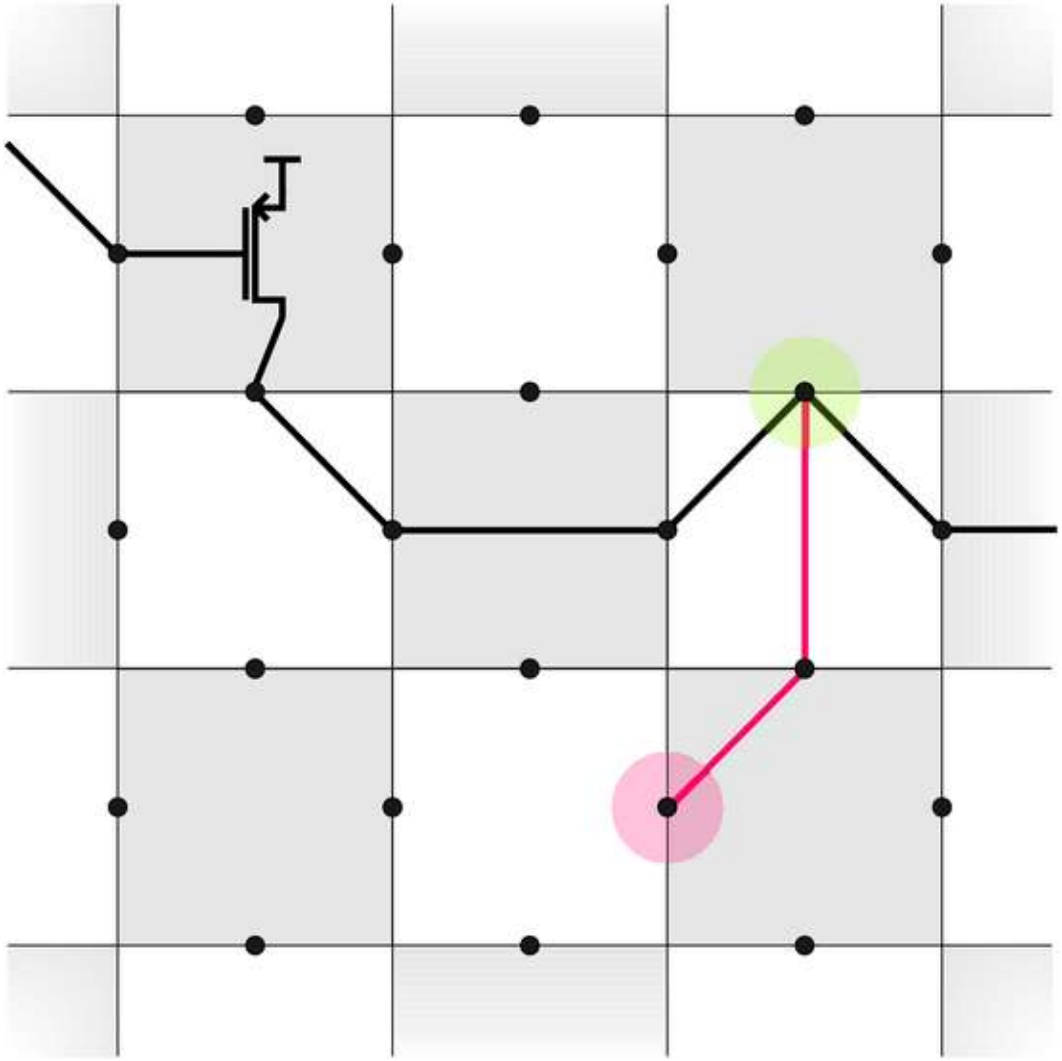
- select start

Turtle GA : Mutation



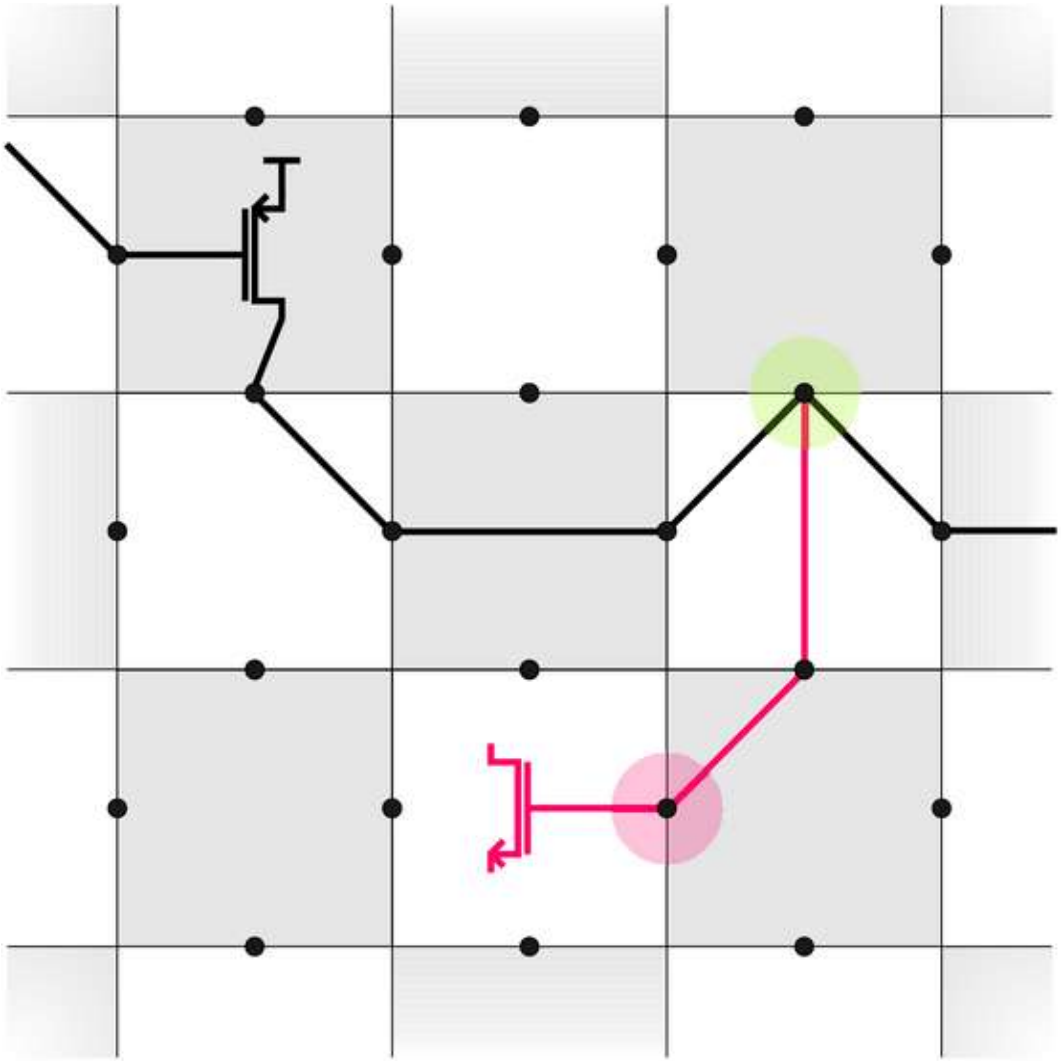
- select start
- create wire

Turtle GA : Mutation



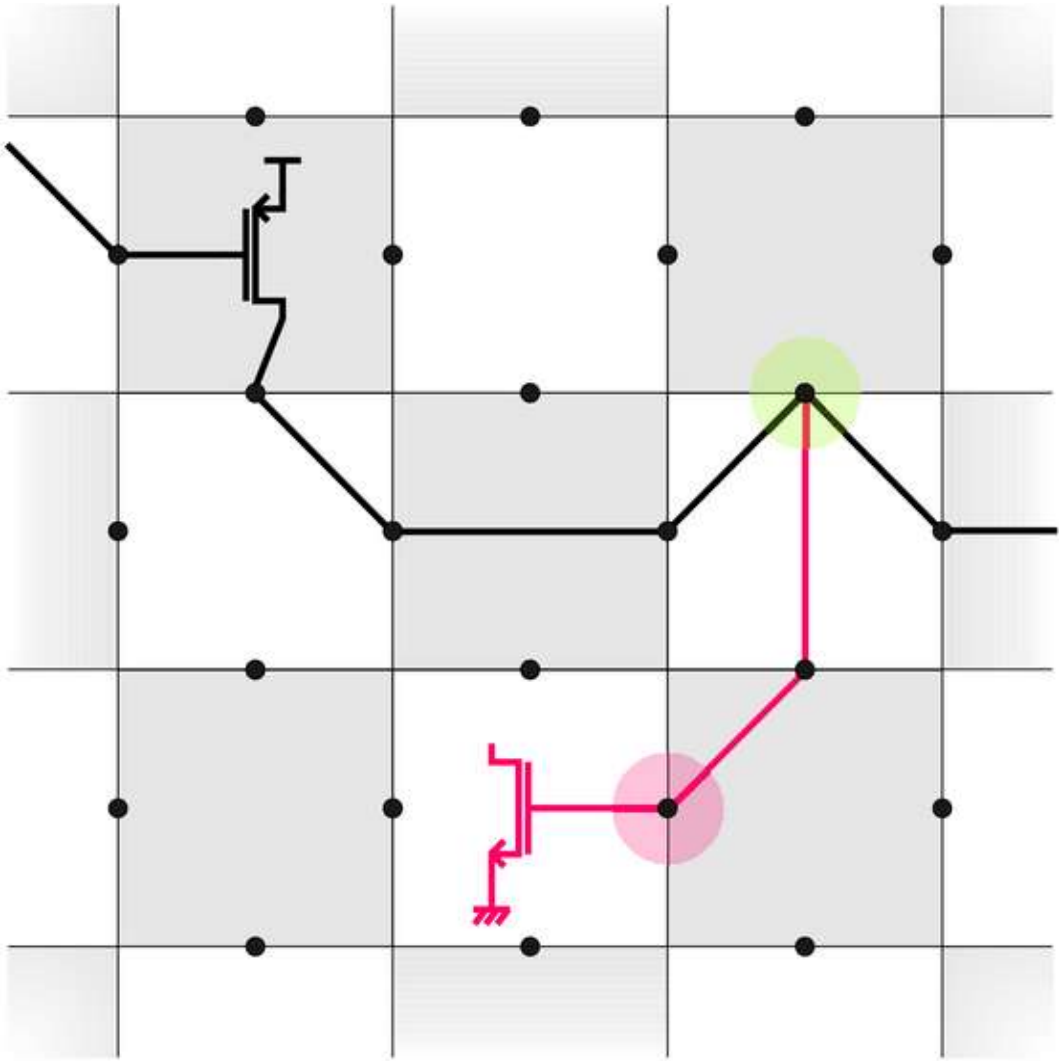
- select start
- create wire

Turtle GA : Mutation



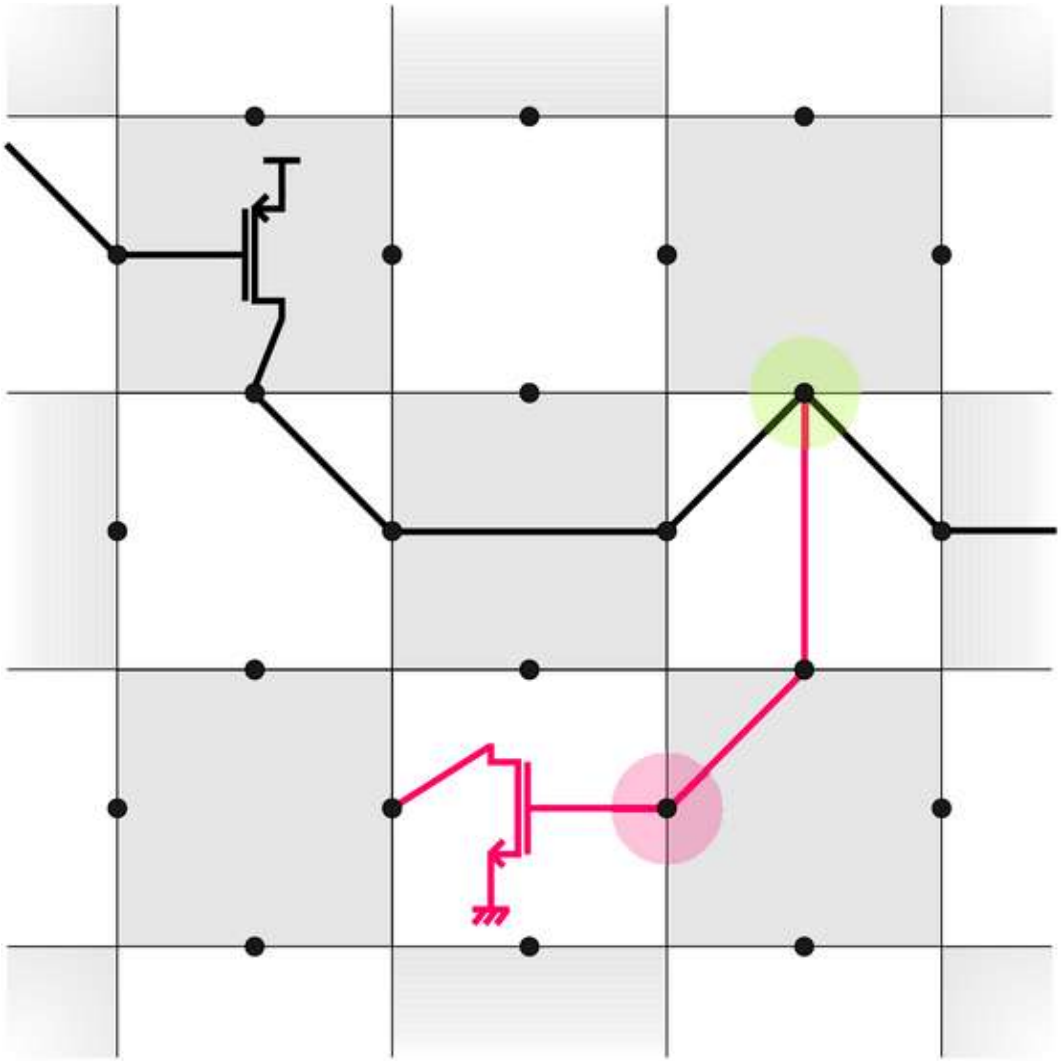
- select start
- create wire
- create transistor

Turtle GA : Mutation



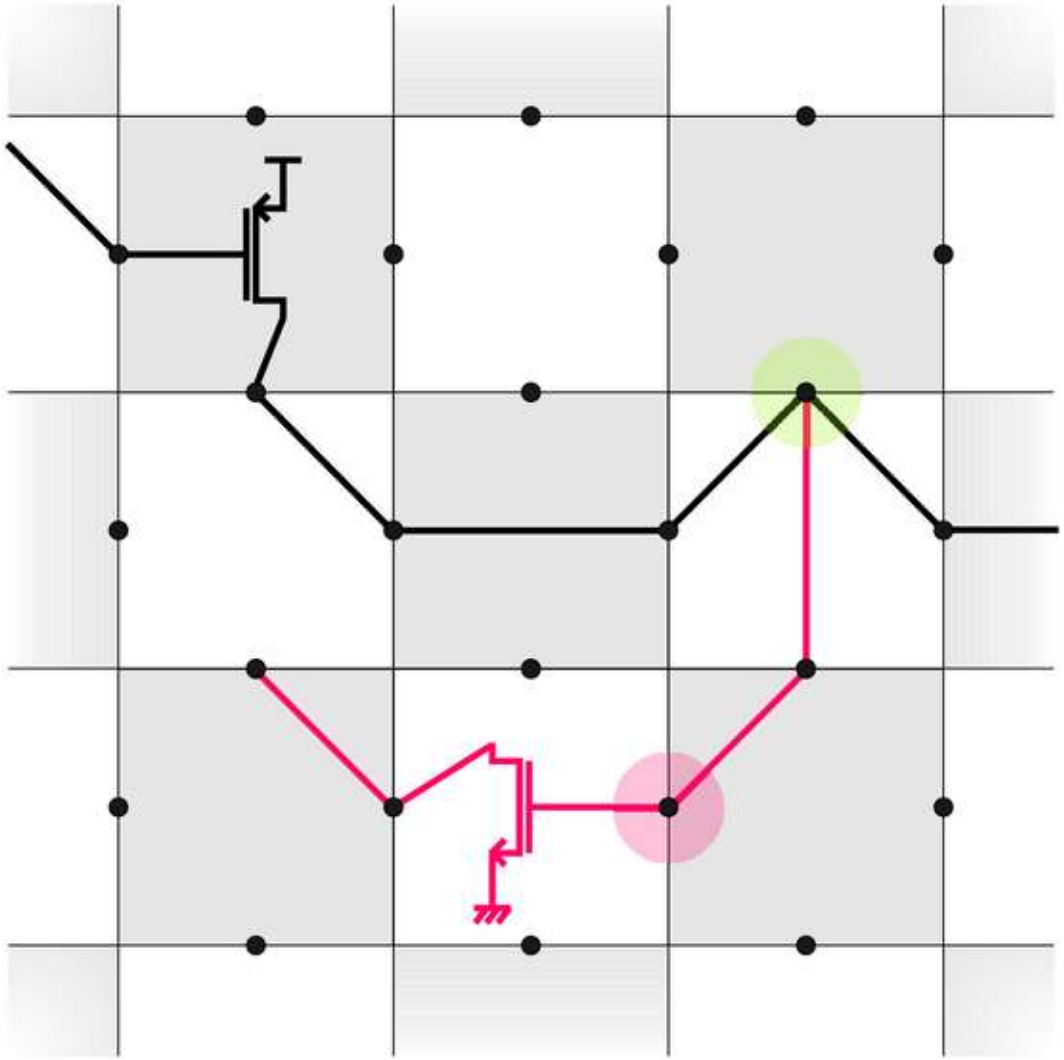
- select start
- create wire
- create transistor

Turtle GA : Mutation



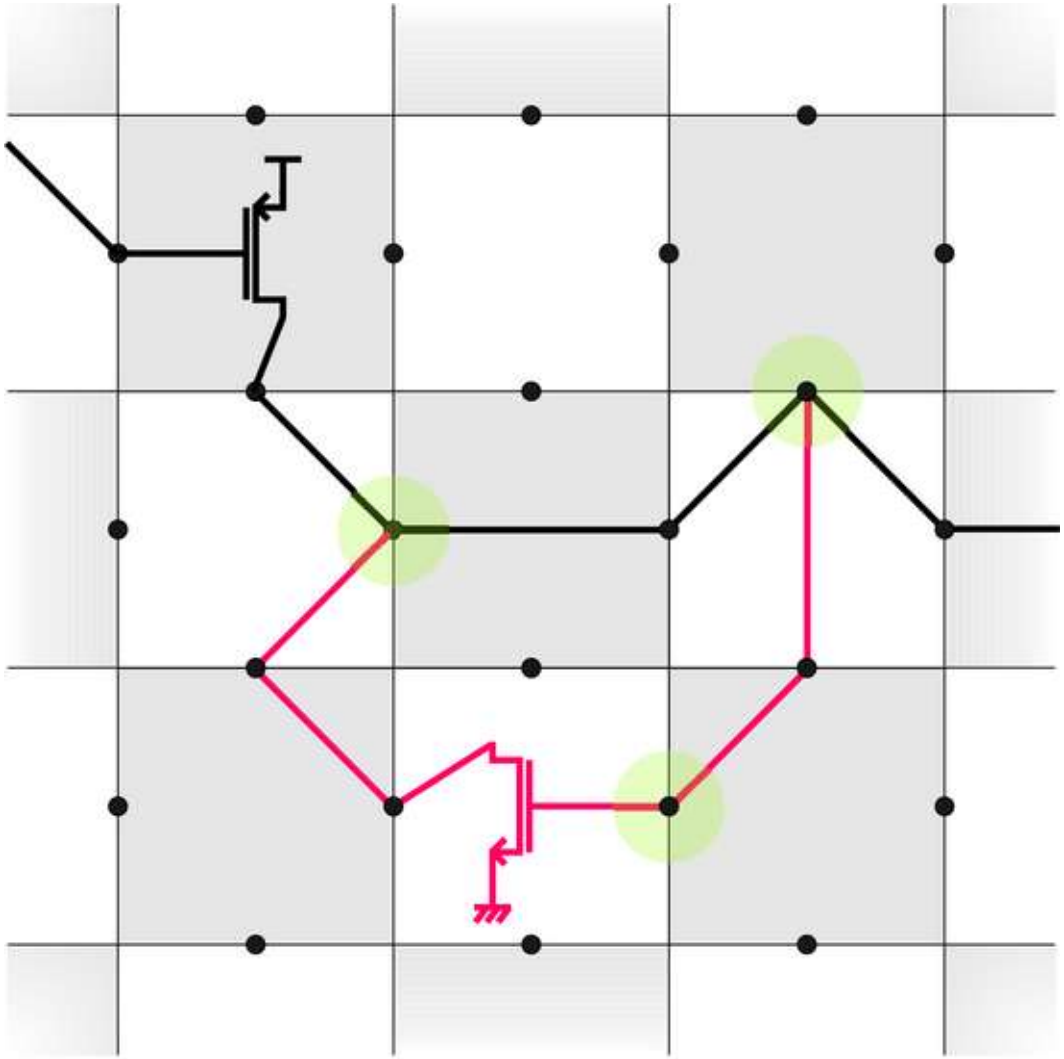
- select start
- create wire
- create transistor

Turtle GA : Mutation



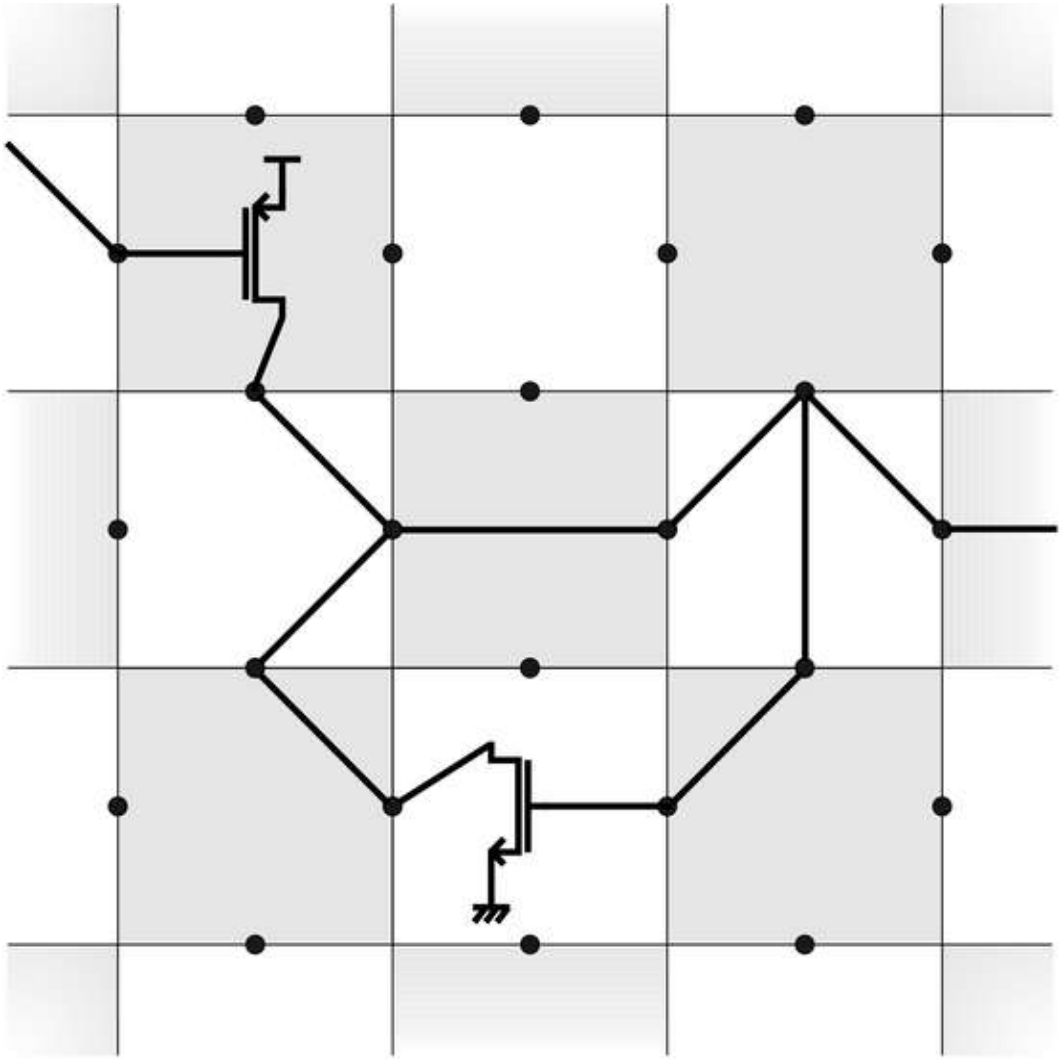
- select start
- create wire
- create transistor

Turtle GA : Mutation

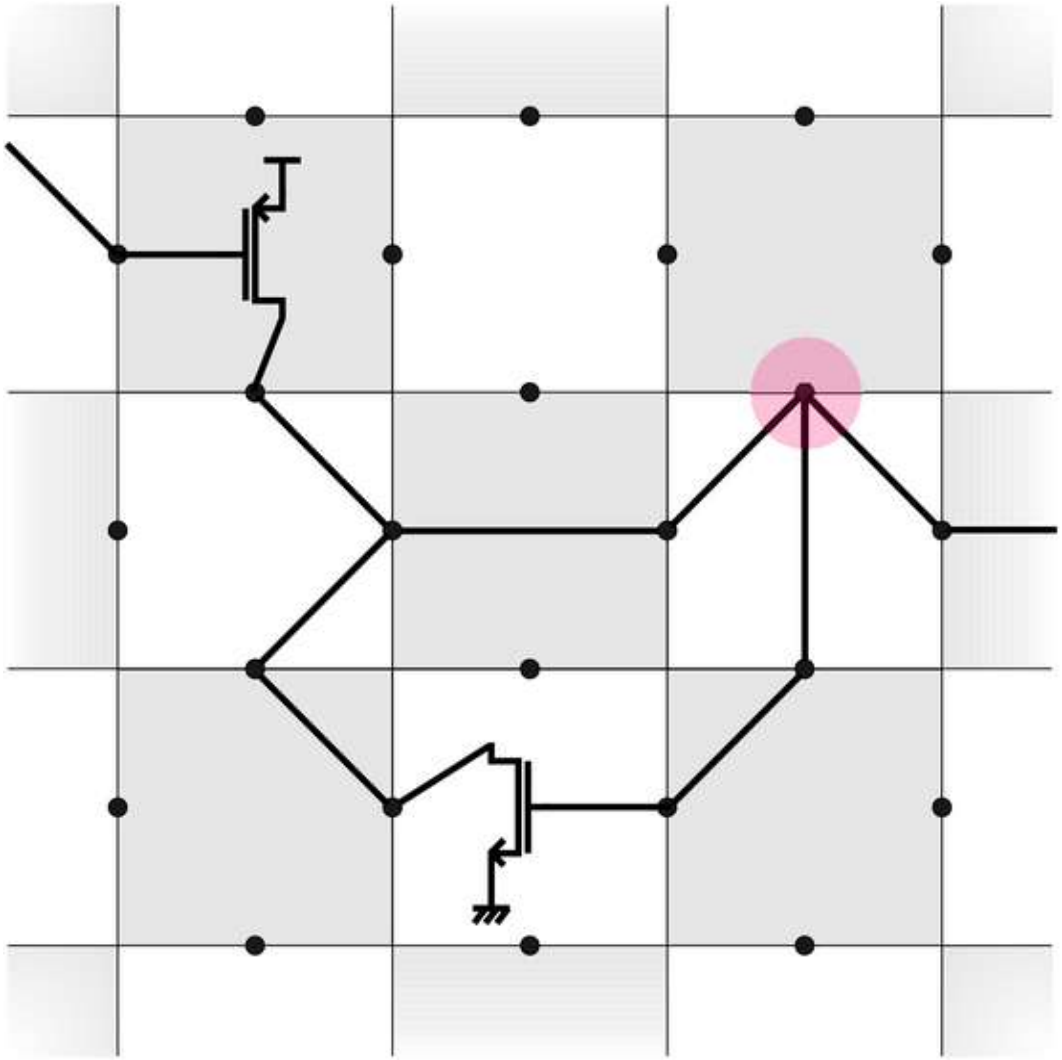


- select start
- create wire
- create transistor
- validate

Turtle GA : Mutation

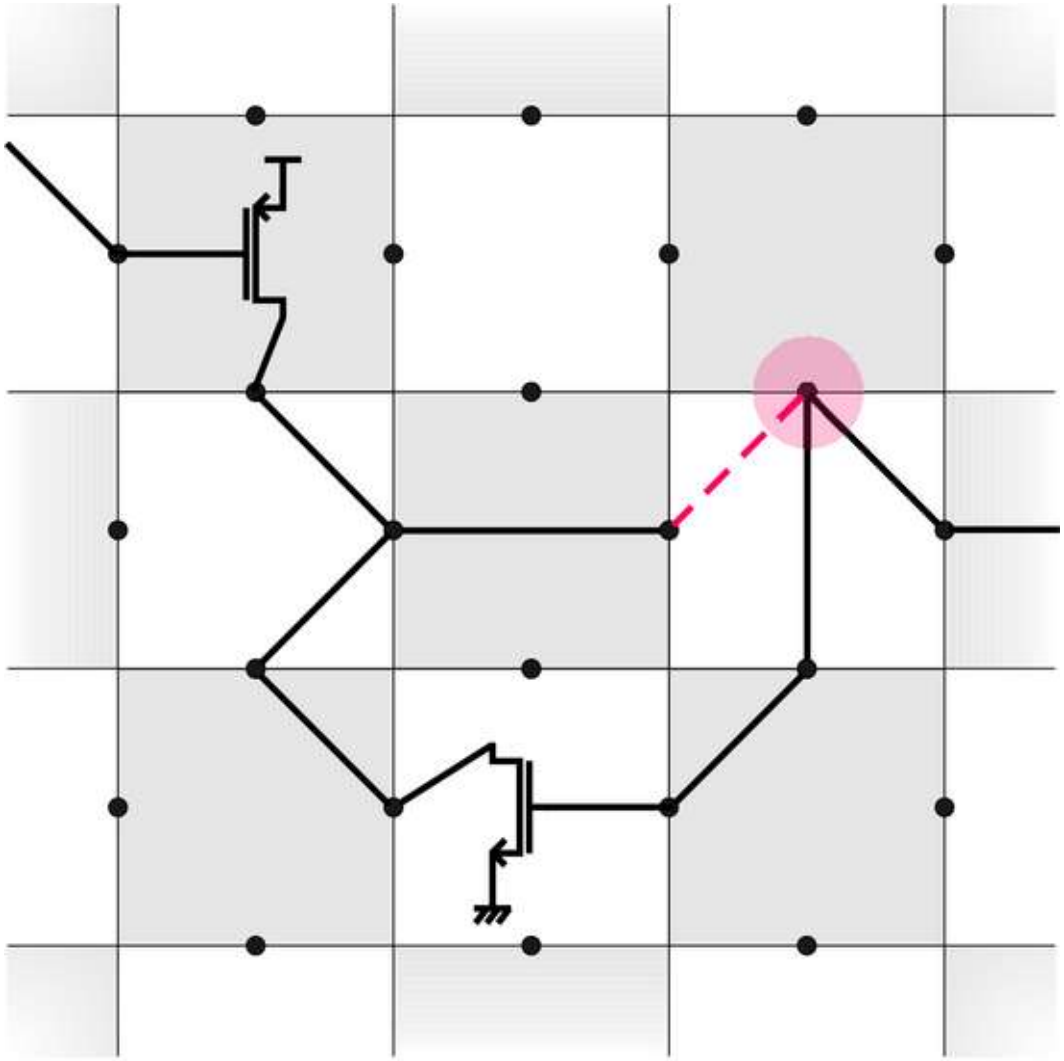


Turtle GA : Mutation



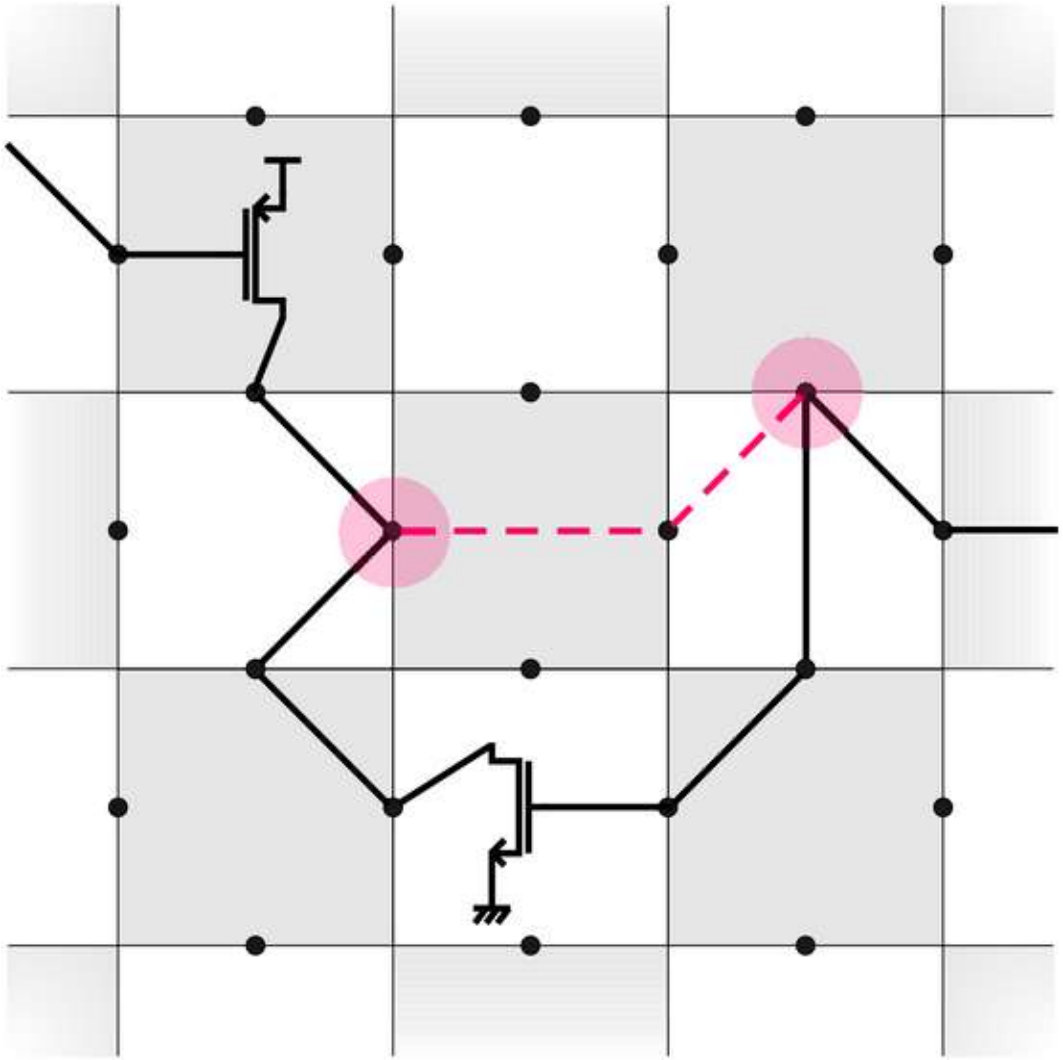
- select start

Turtle GA : Mutation



- select start
- erase wire

Turtle GA : Mutation



- select start
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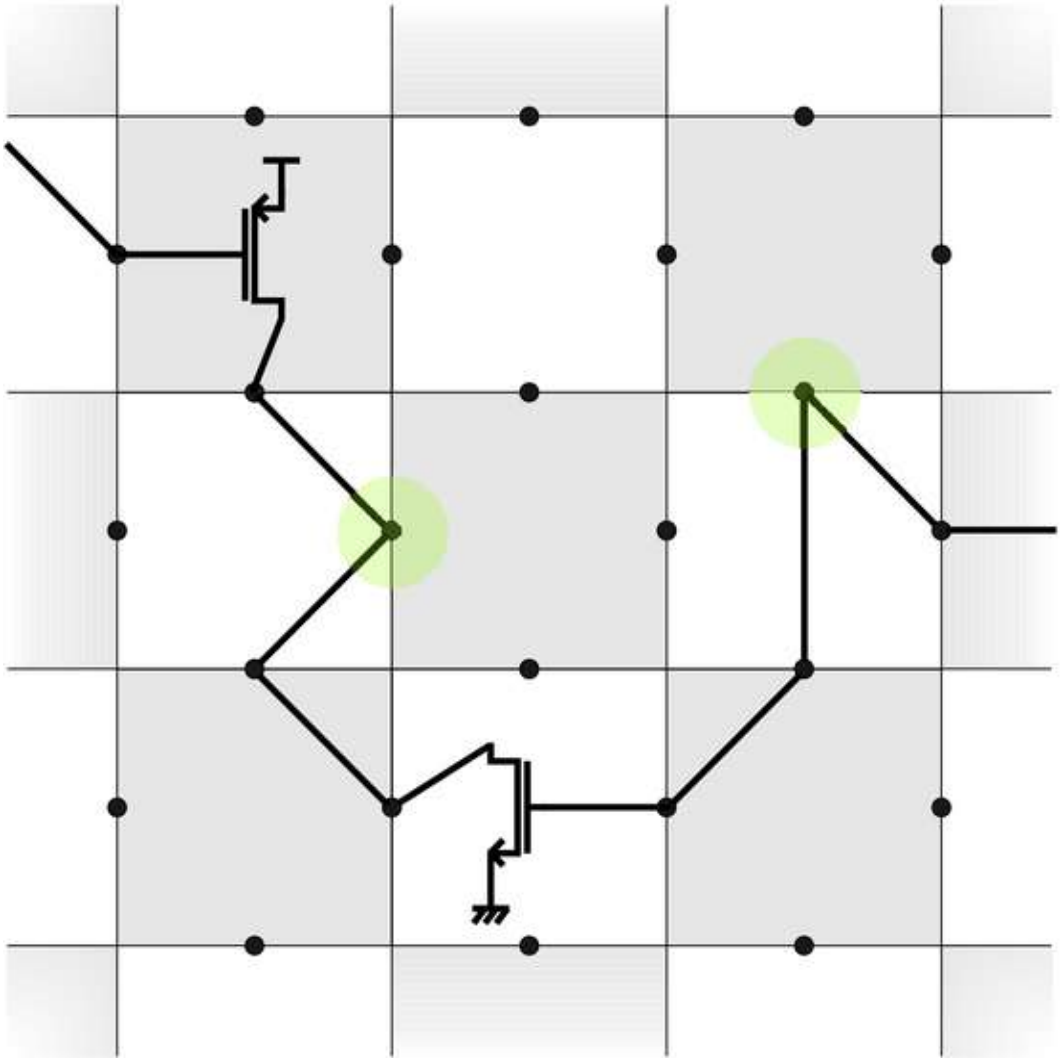
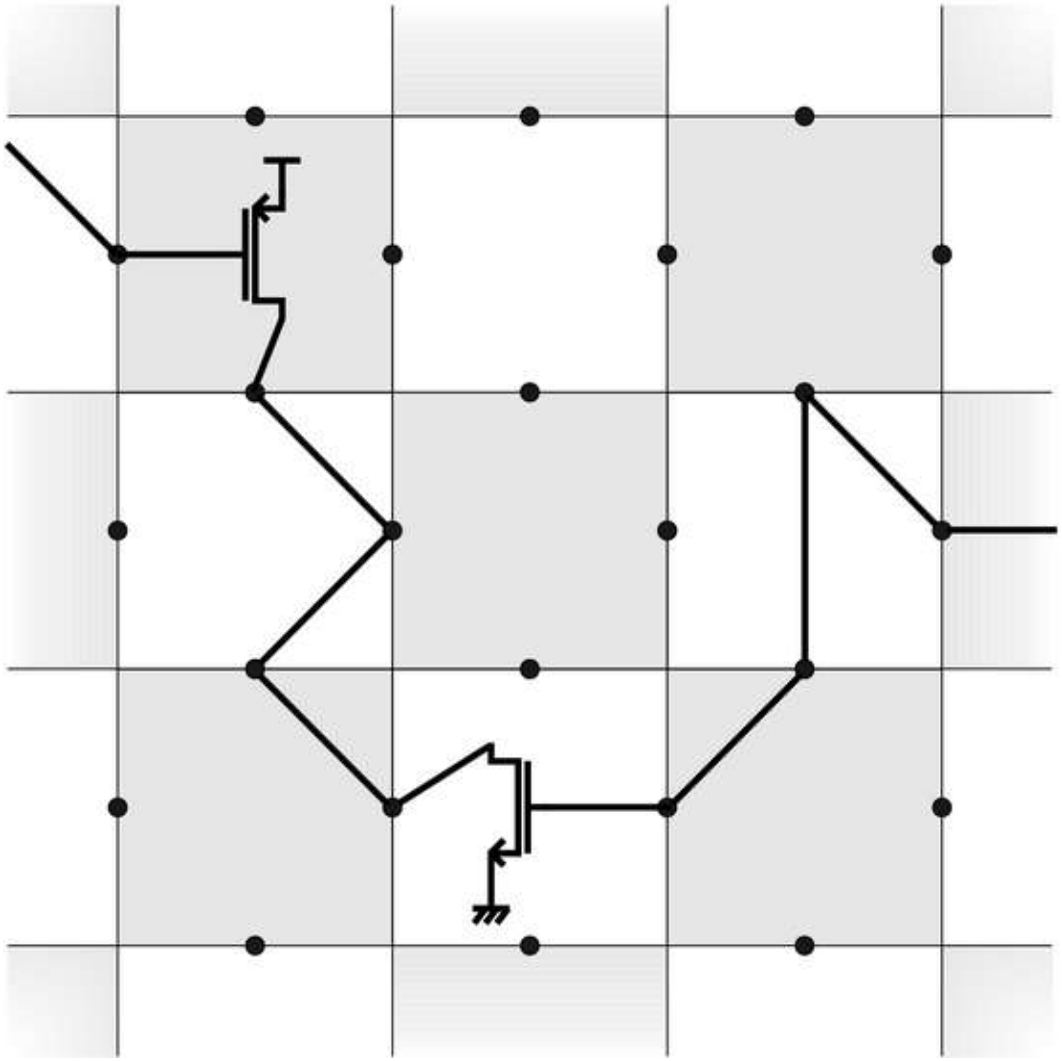
Turtle GA : Mutation



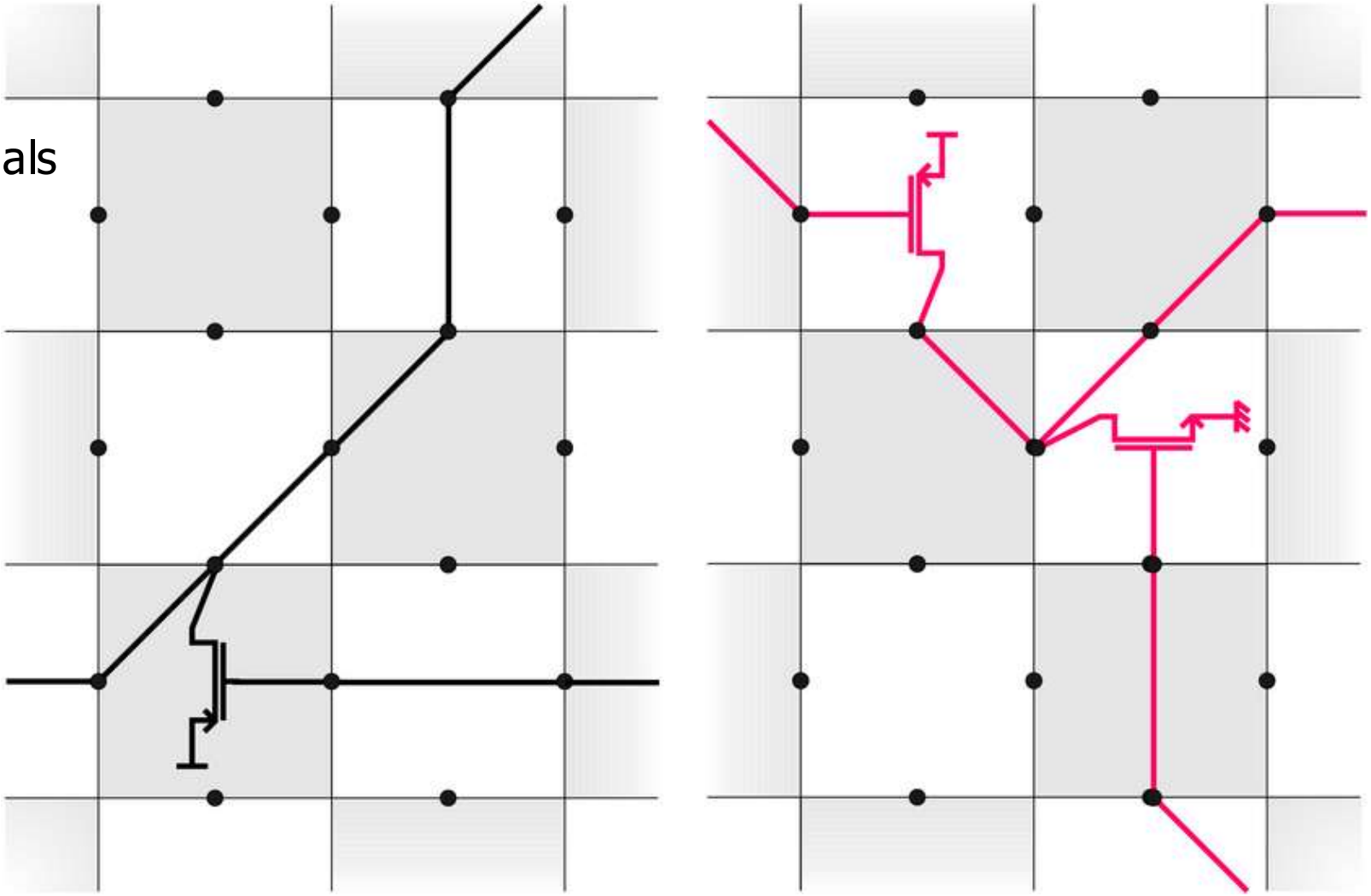
- select start
- erase wire
- validate

Turtle GA : Mutation



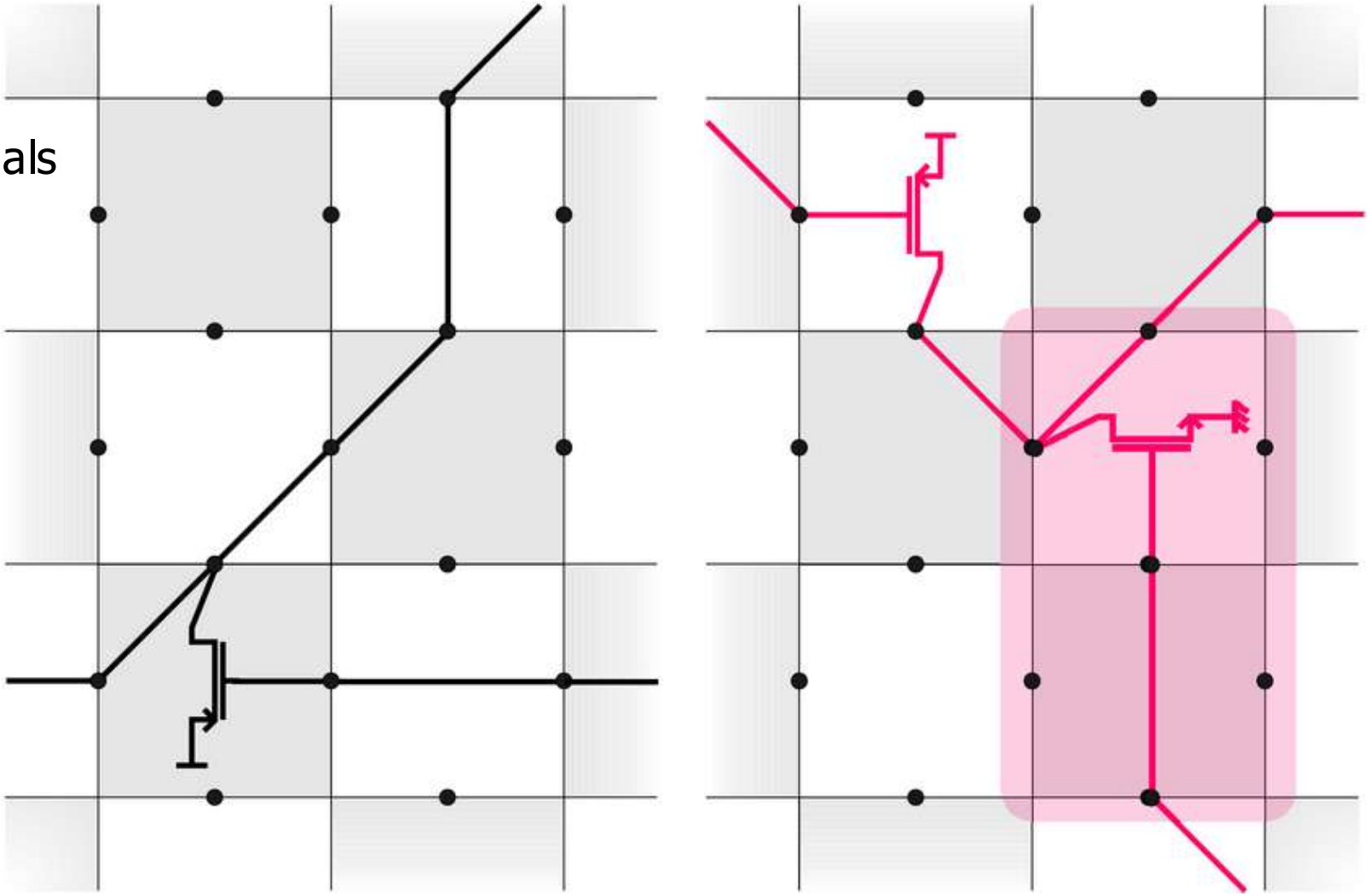
Basic GA : Crossover

- select individuals



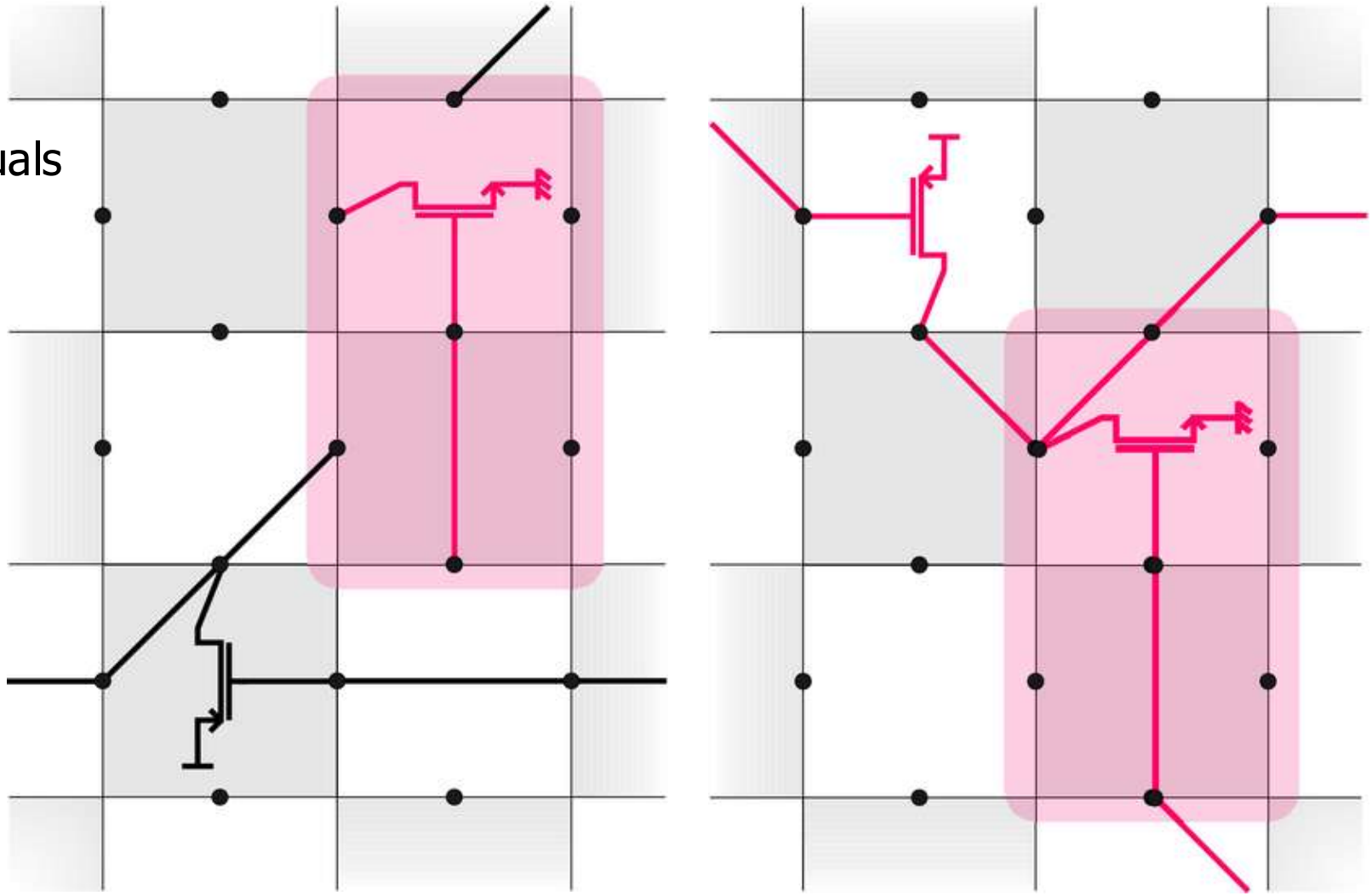
Basic GA : Crossover

- select individuals
- select block

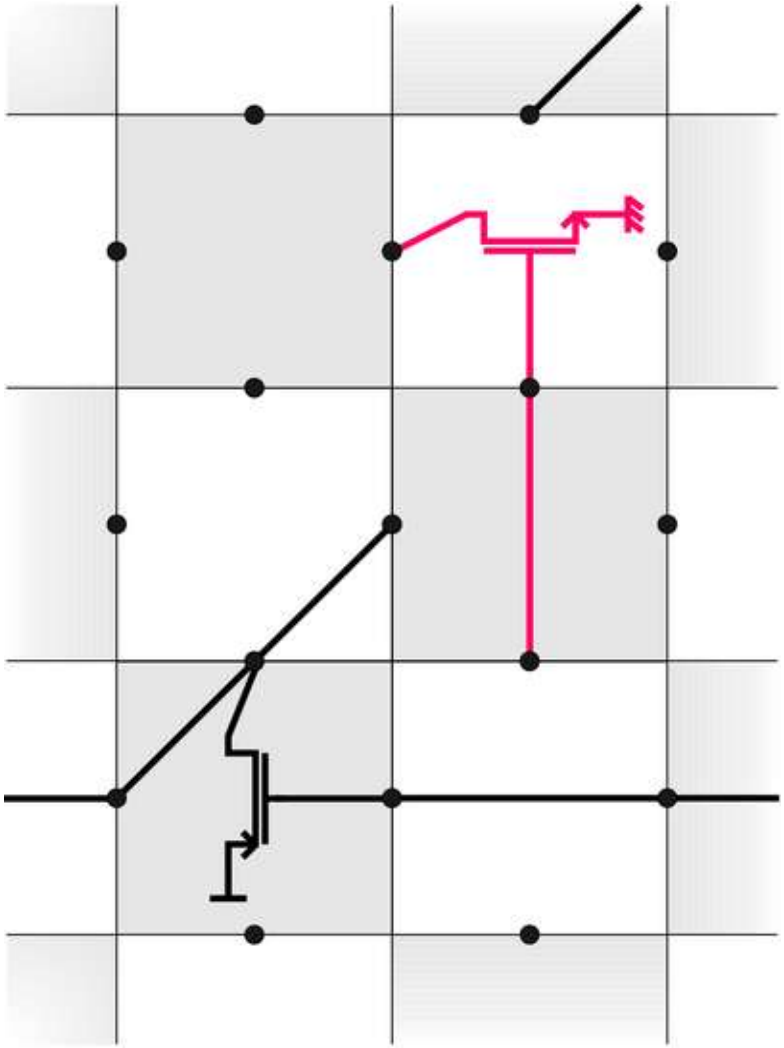


Basic GA : Crossover

- select individuals
- select block
- copy block

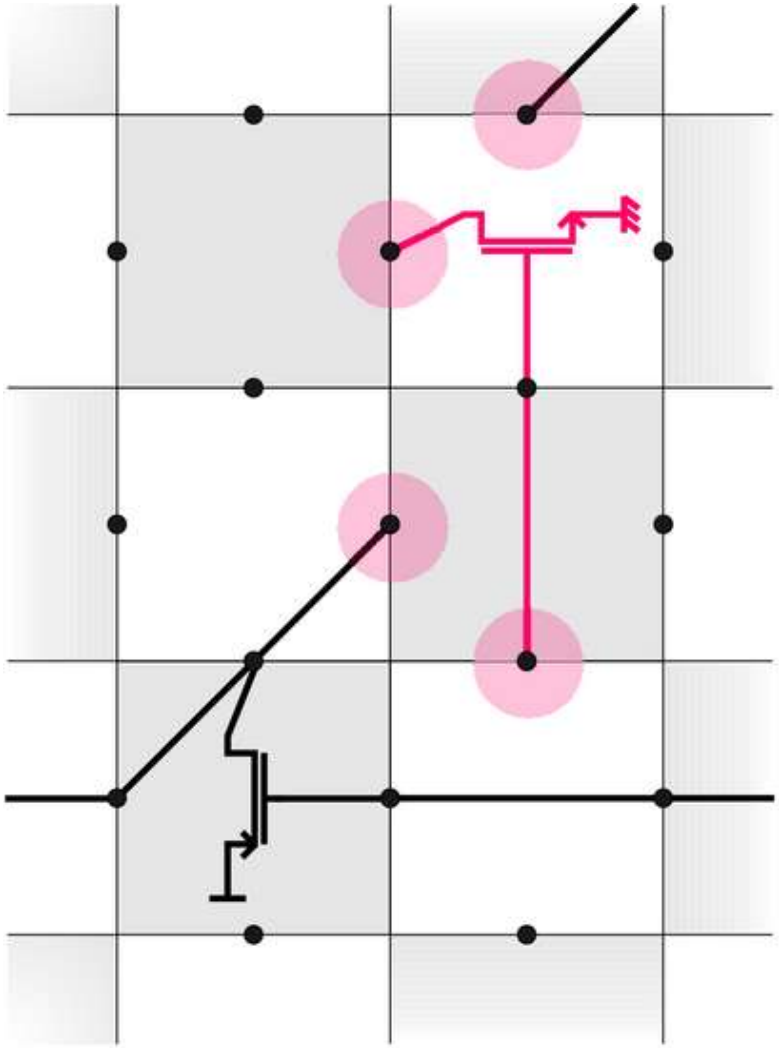


Basic GA : Crossover



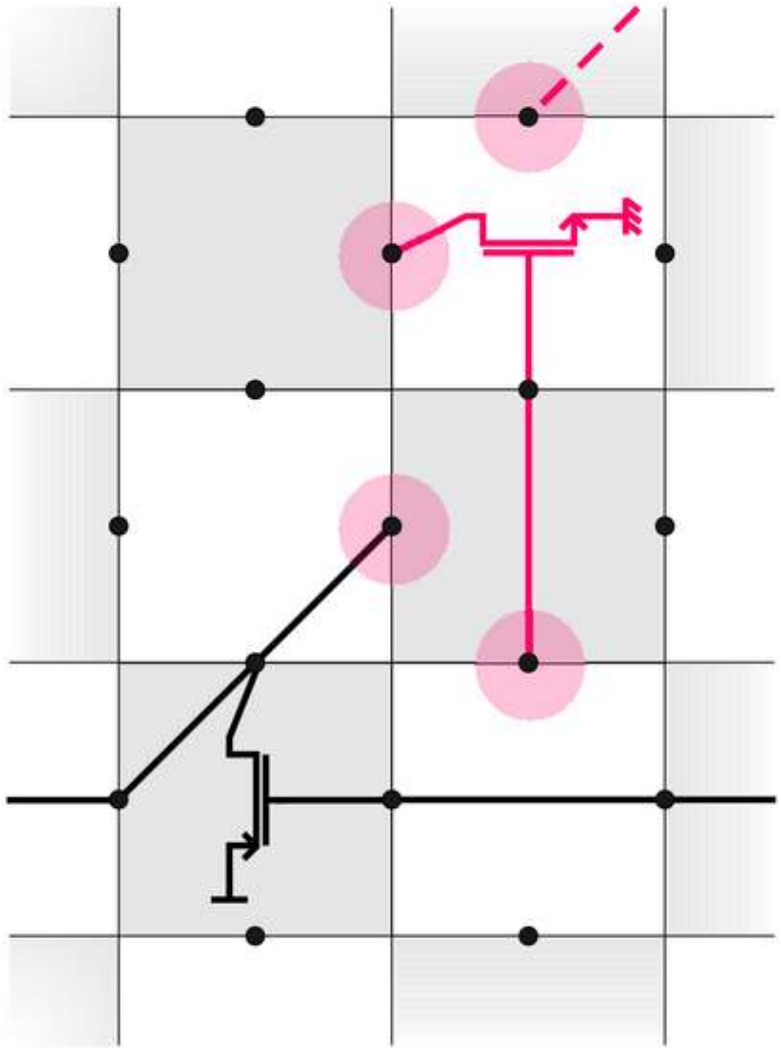
Problems:
- floating nodes
- no transfer

Turtle GA : Crossover Implant



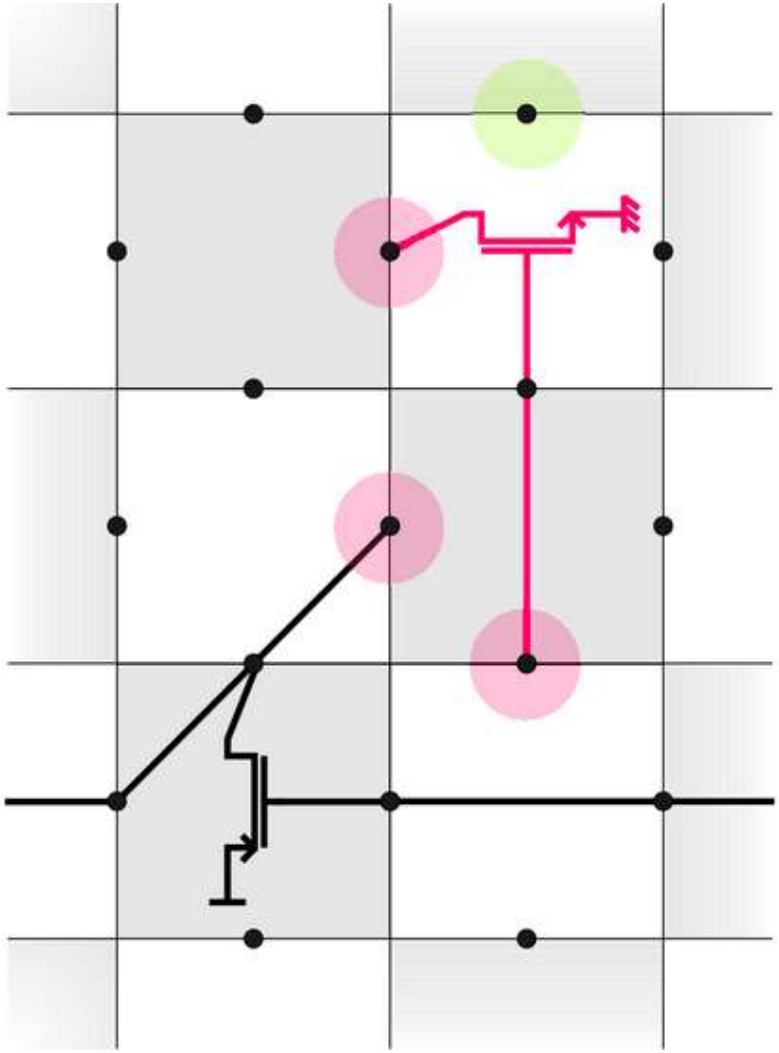
- connect floating nodes

Turtle GA : Crossover Implant



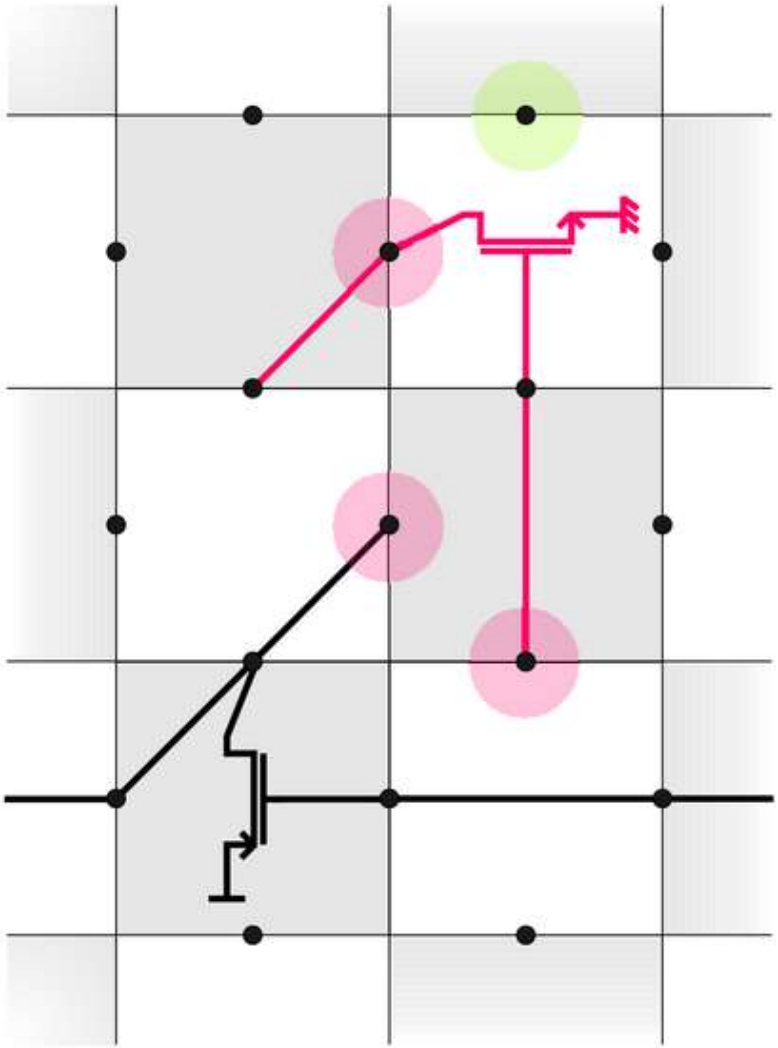
- connect floating nodes

Turtle GA : Crossover Implant



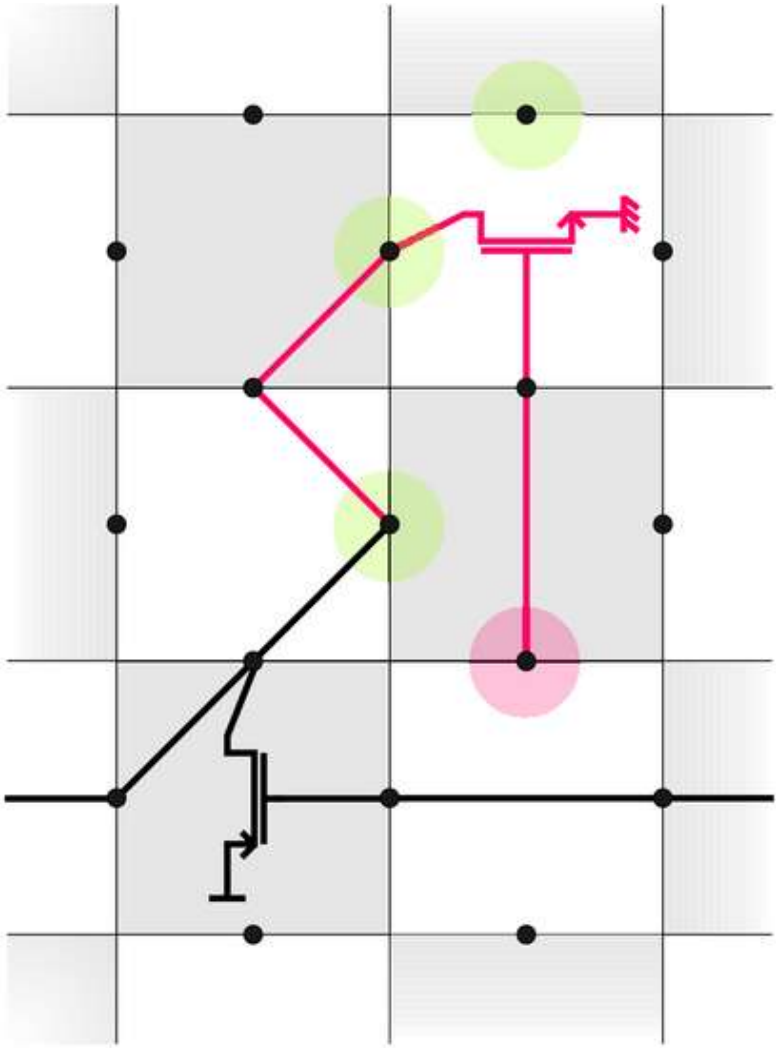
- connect floating nodes

Turtle GA : Crossover Implant



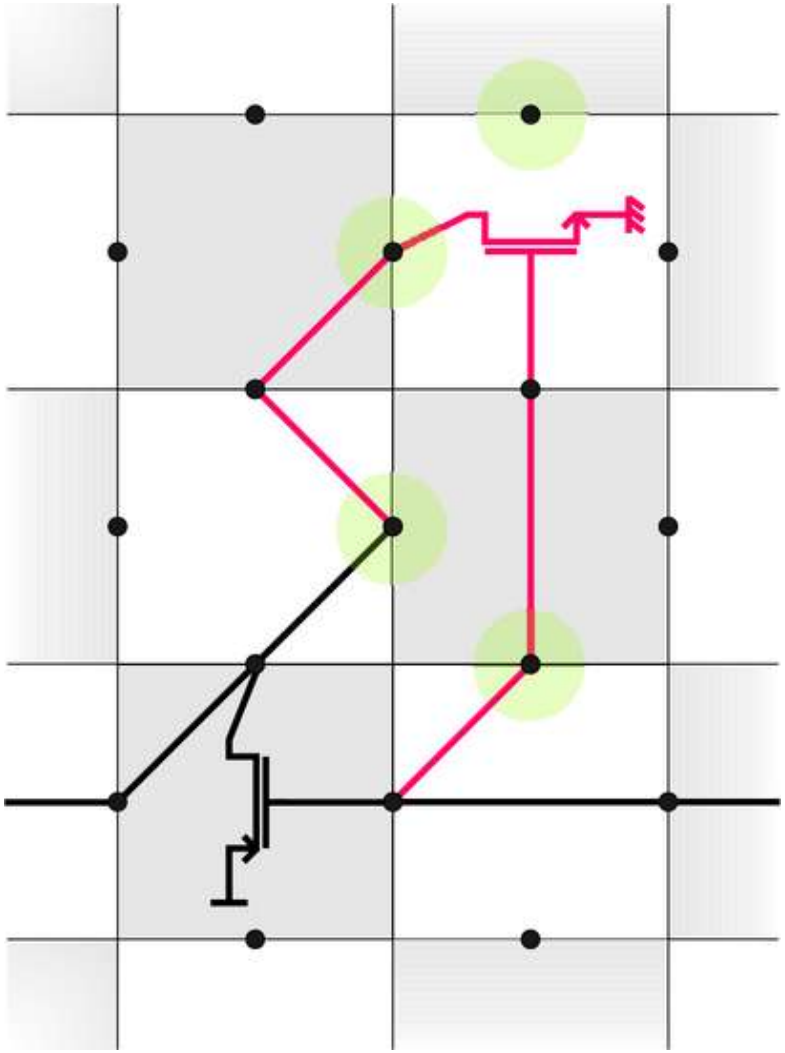
- connect floating nodes

Turtle GA : Crossover Implant



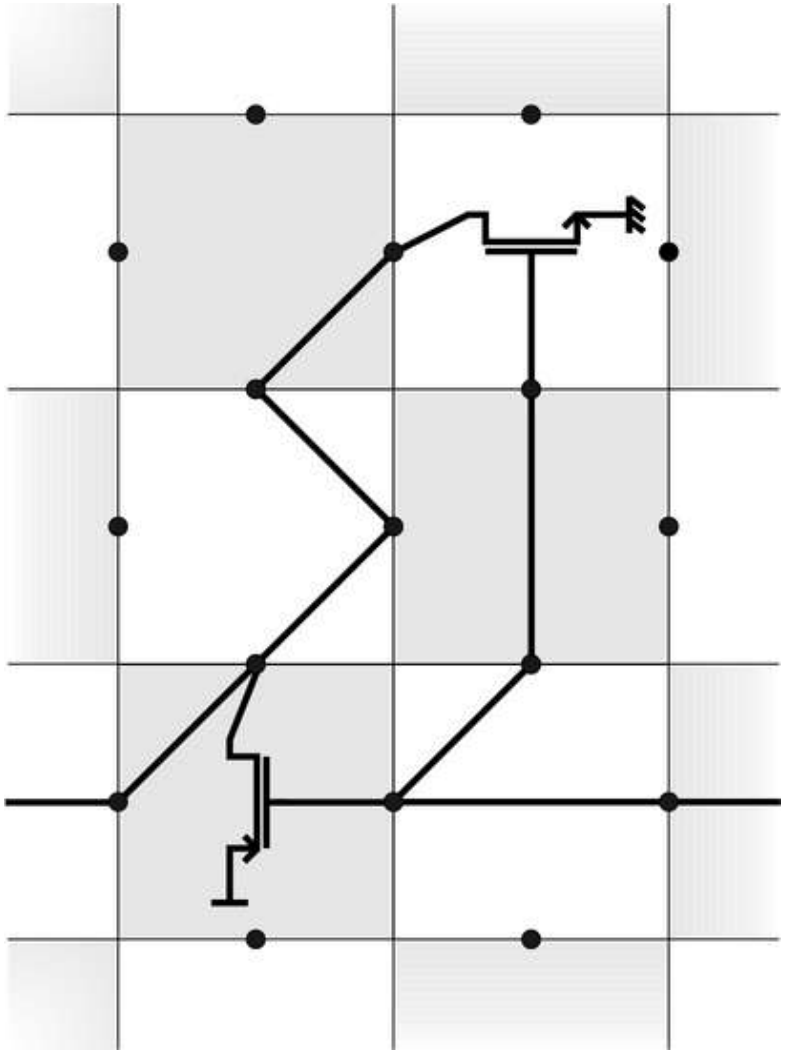
- connect floating nodes

Turtle GA : Crossover Implant

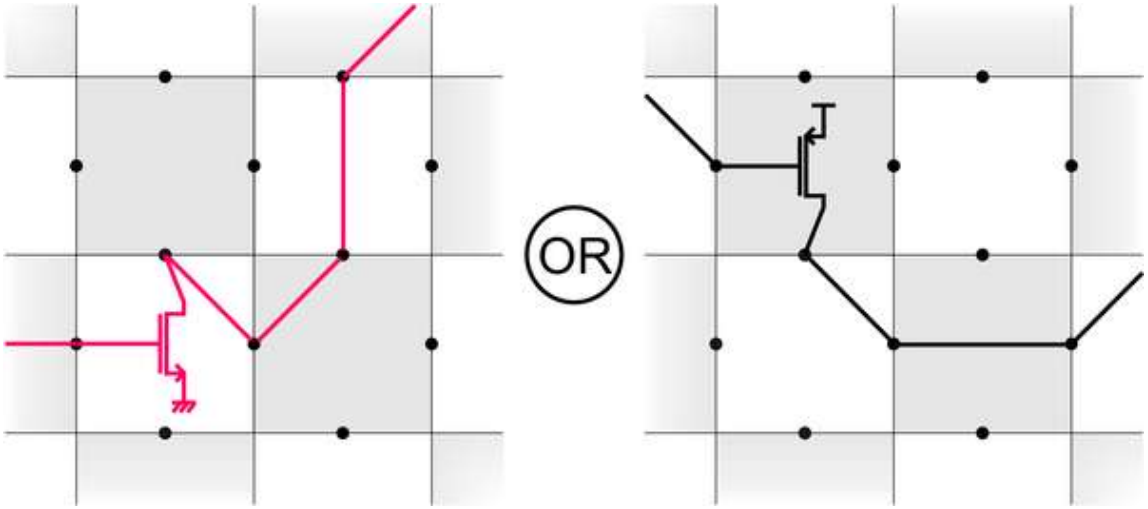


- connect floating nodes
- validate

Turtle GA : Crossover Implant

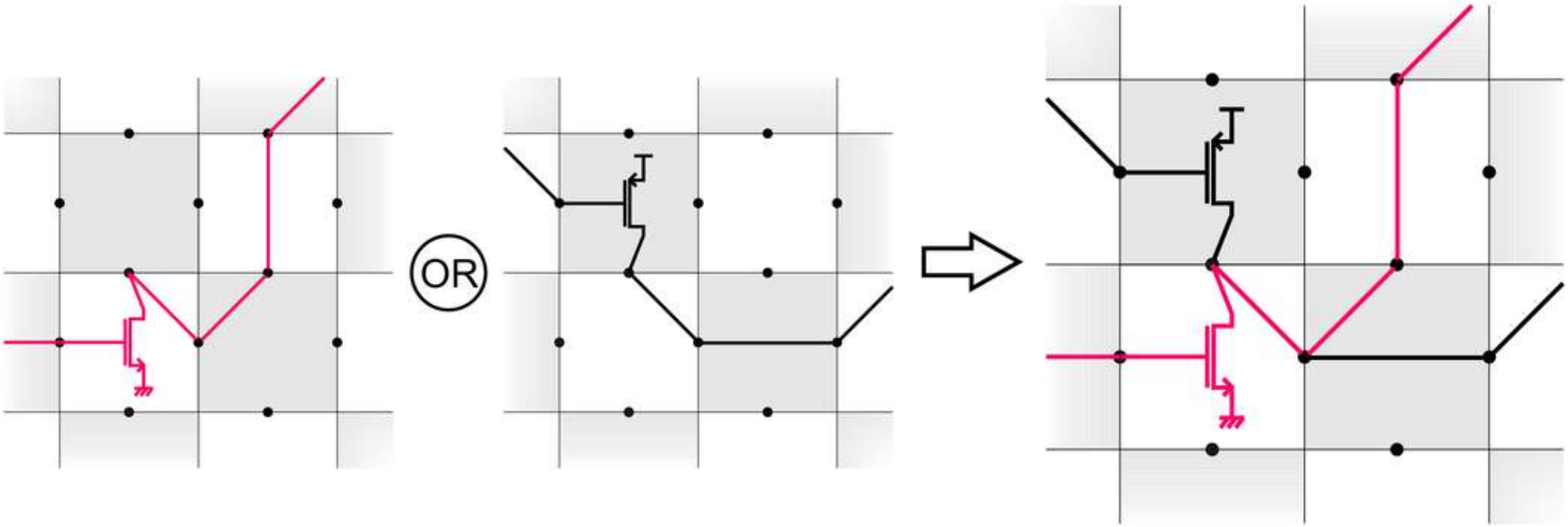


Turtle GA : Crossover OR



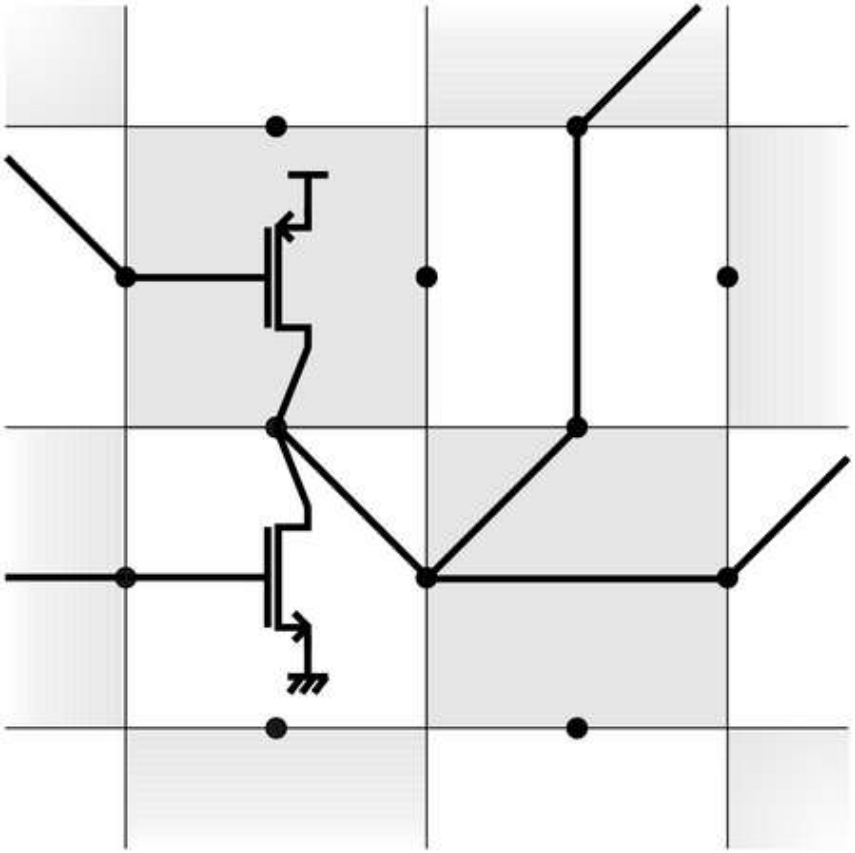
- select two individuals

Turtle GA : Crossover OR



- select two individuals
- calculate logic OR

Turtle GA : Crossover OR



Experimental Setup : GA

- 50 individuals / 20k generations
- 30 evolution runs / experiment
- tournament selection (size 7) – no elitism
- mutation / crossover rates $\propto$ best fitness
- comparator: 7x7 FPTA cells
- gates: 8x8 transistor cells
- 2 inputs, 1 output

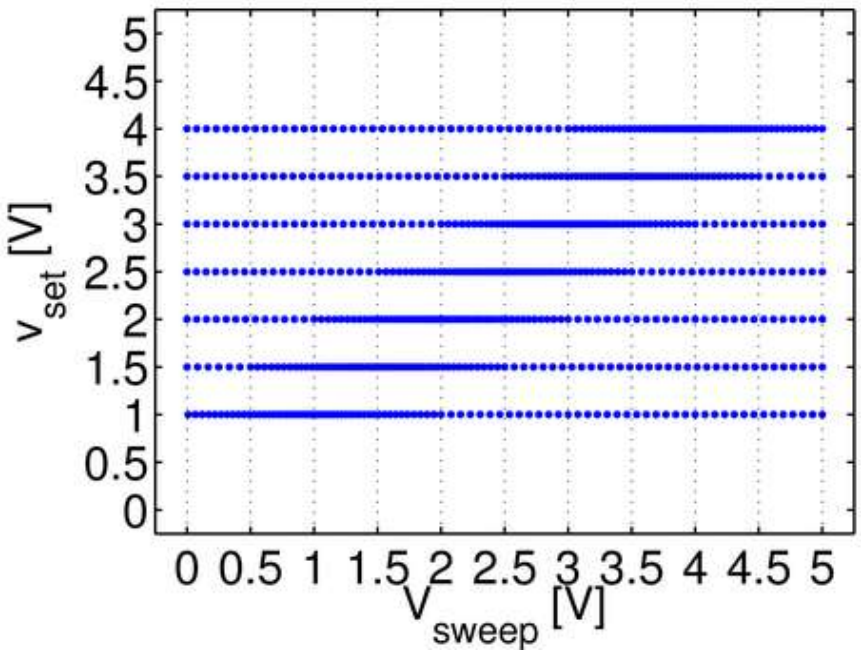
GA Parameter	Basic GA	Turtle GA
mutation rate	4 ... 0.8 %	1.25 ... 0.25 %
crossover rate	1 ... 0.2 %	1 ... 0.2 %
max. cross. block size	4 x 4	4 x 4

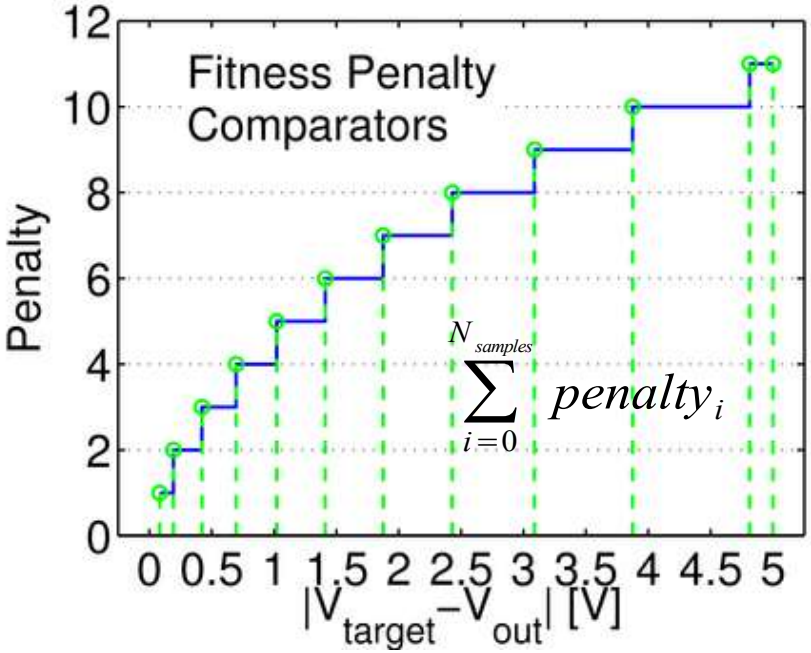
Experimental Setup : Simulation

- simulator: SPICE3f5
- resistance of the switches represented by mean values: source, drain: 330 Ohm; gate: 2,3 kOhm

- circuits are evolved on hardware
- SPICE netlist generation
- simulation outside the FPTA using spice3f5

Comparators : Setup





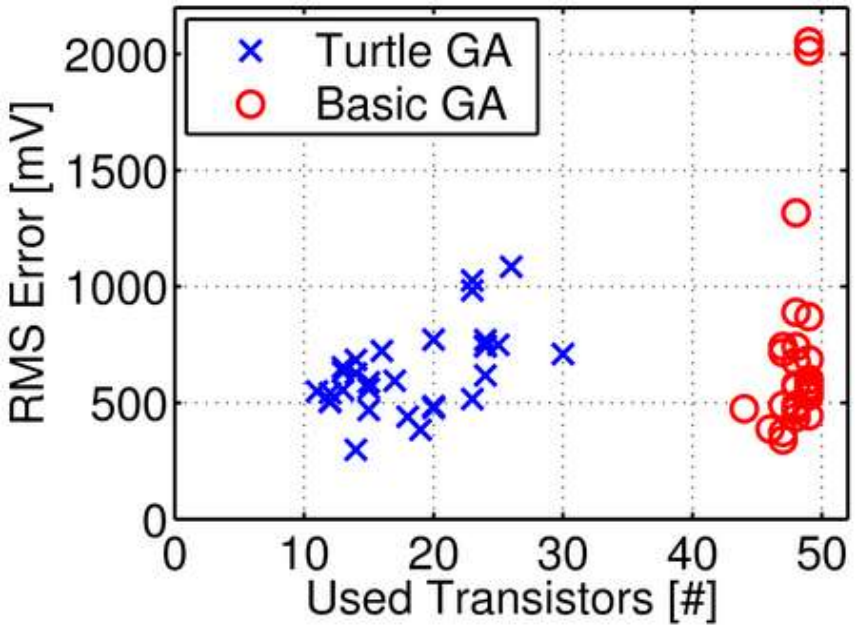
- a set of 7 curves (Vset)
- each with 90 sample voltages (Vsweep)

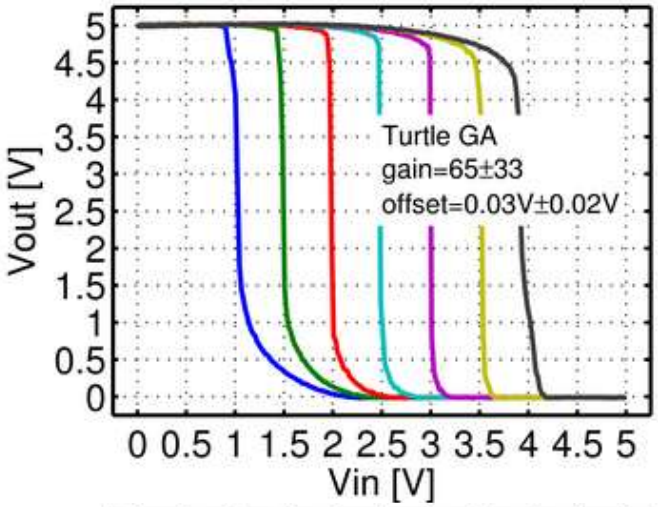
$$V_{Out} = \begin{cases} V_{set} \leq V_{sweep} & : \ 0\,V \\ V_{set} > V_{sweep} & : \ 5\,V \end{cases}$$

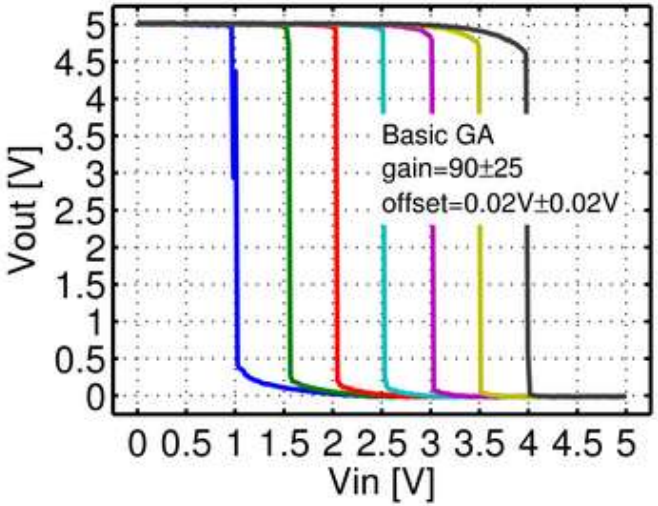
- a discrete fitness function -> minimize noise and fluctuations of the analog output

Comparators : Comparison of Both GAs

- both algorithms perform equally well
- Basic GA achieved a slightly higher gain
- Turtle GA reduces resource consumption

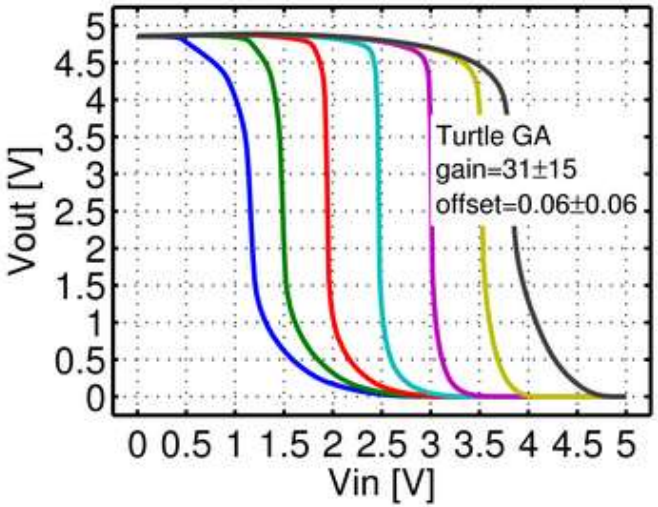


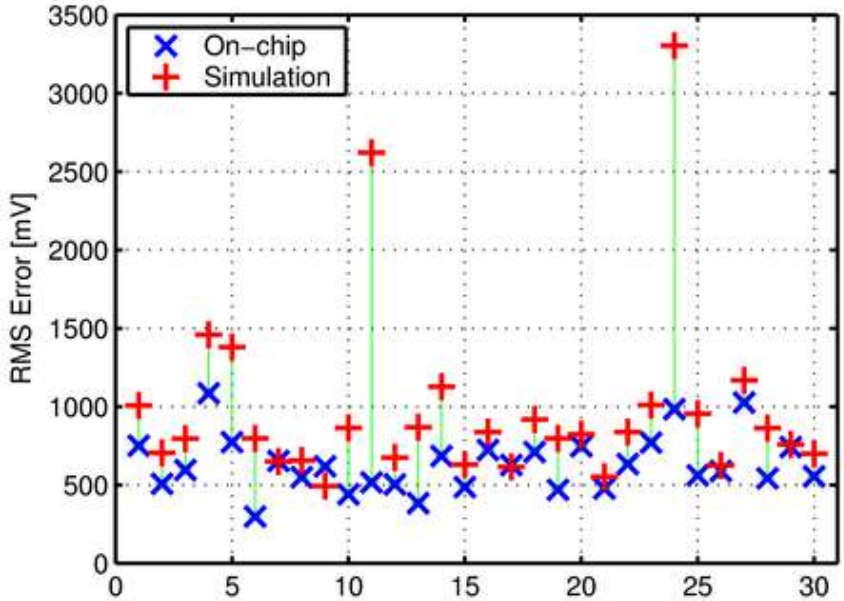




Comparators : Simulation Results

- two circuits fail in simulation
- mean performance is slightly worse than on the FPTA
- best circuits perform equally well

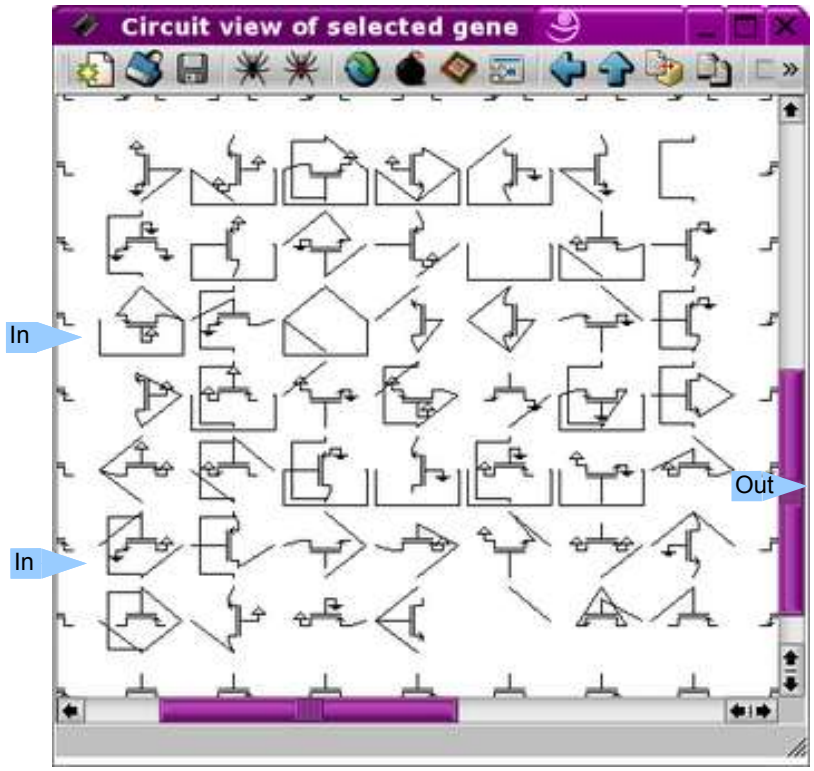




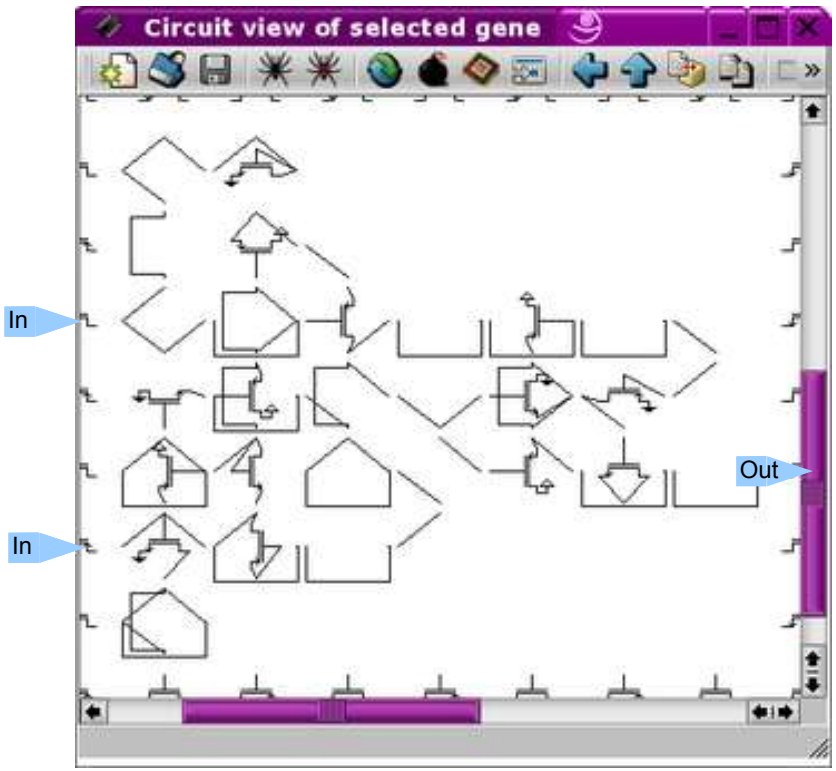
Promising:
A complex circuit has been proven to work as well in simulation

Towards an “Understandable” Phenotype

Basic GA



Turtle GA

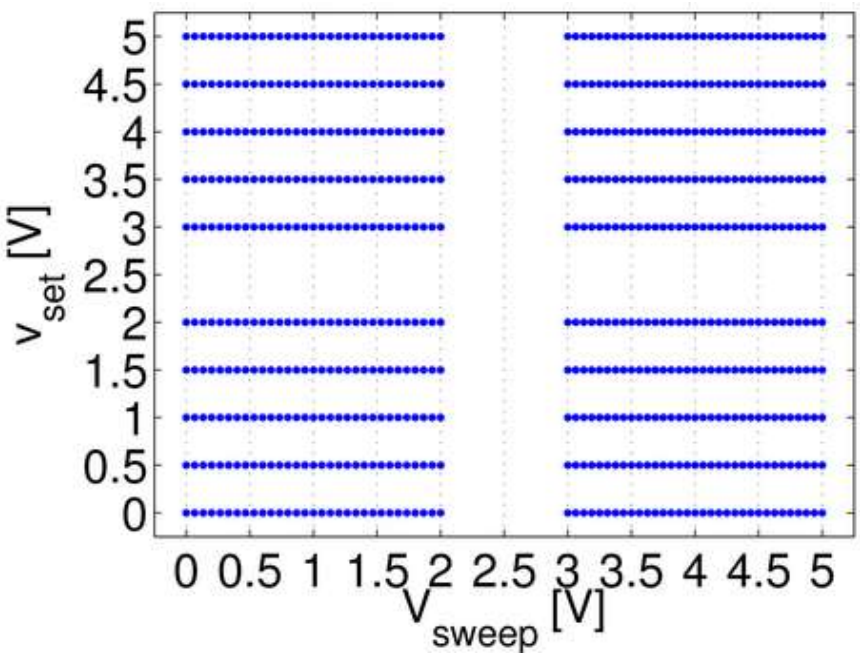


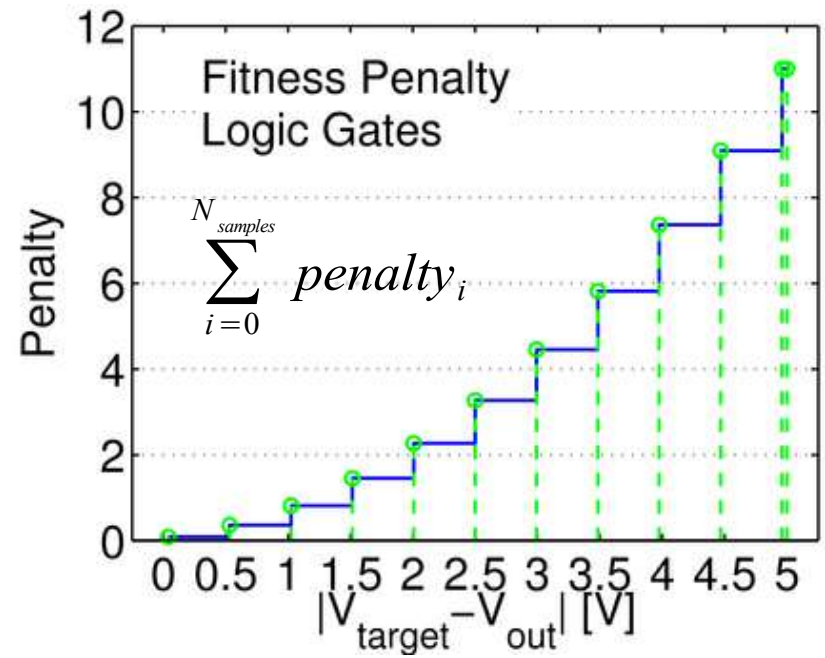
- not connected transistors are hidden

Gates : Setup

- a set of 10 curves (Vset)
- each with 64 sample voltage (Vsweep)
- transition region is omitted

$$V_{Out} = \begin{cases} (V_{set} \wedge V_{sweep}) \cdot 5V \\ (V_{set} \vee V_{sweep}) \cdot 5V \\ (V_{set}\, XOR\, V_{sweep}) \cdot 5V \end{cases}$$

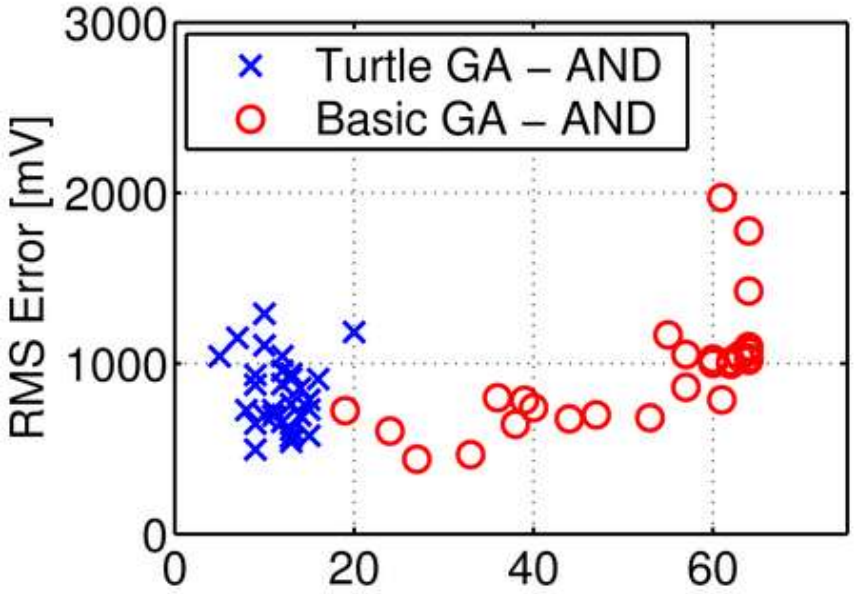


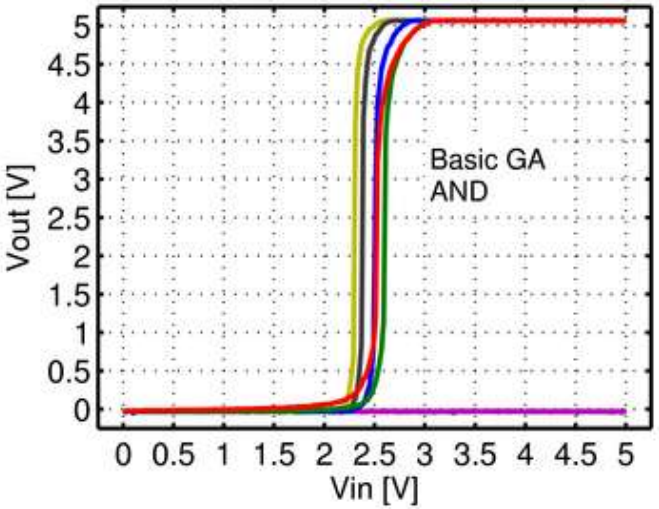


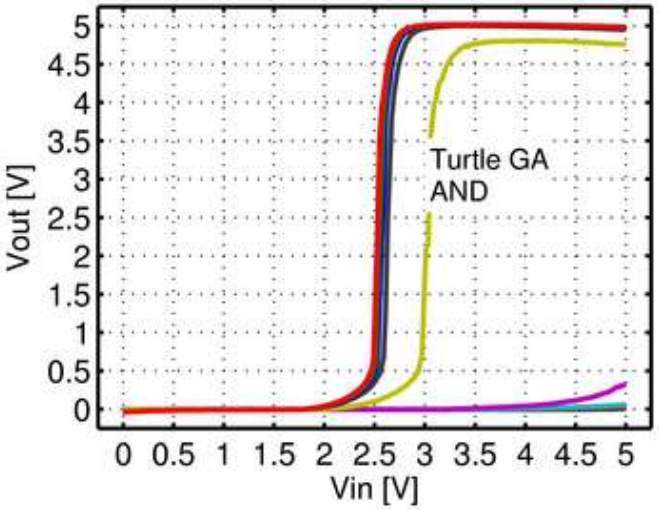
- discrete fitness function -> minimize noise and fluctuations of the analog output

AND Gate : Comparison of Both GAs

- both algorithms find good solutions for the AND
- voltage characteristic looks equally well in both cases
- Turtle GA reduces resource consumption

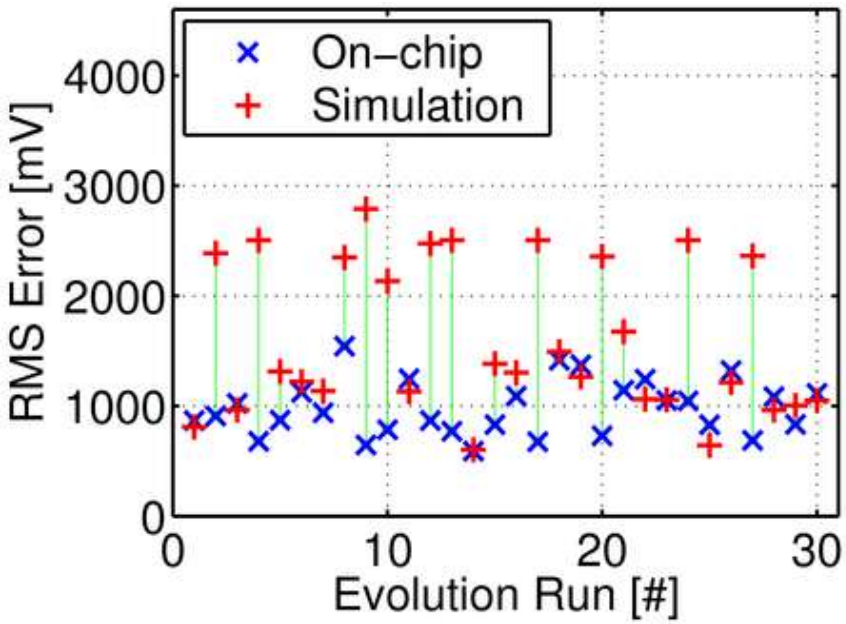


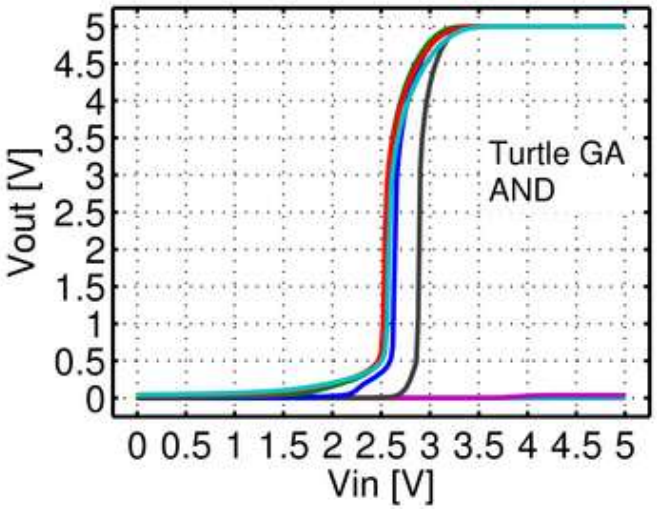




AND Gate : Simulation Results

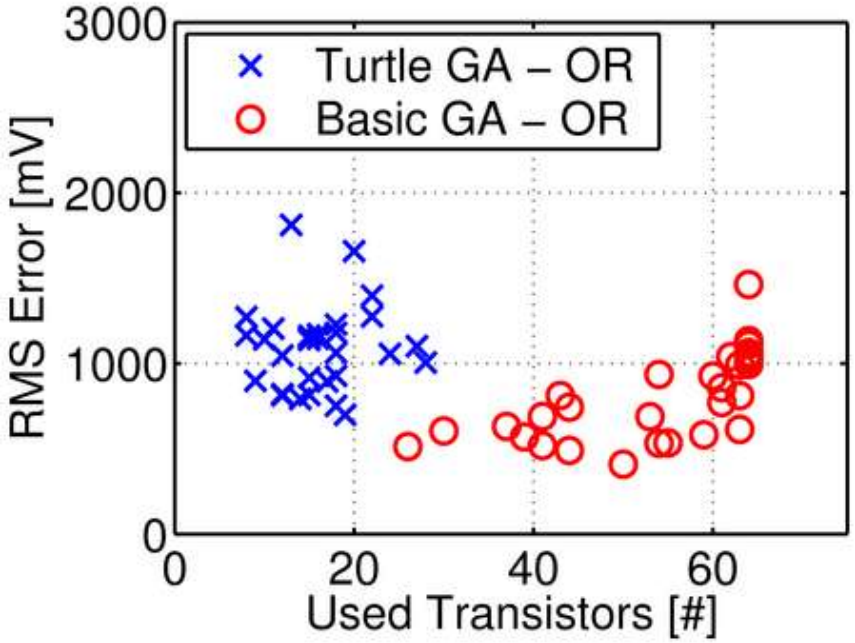
- less than half of the circuits fail in simulation
- best circuits perform equally well as on the chip

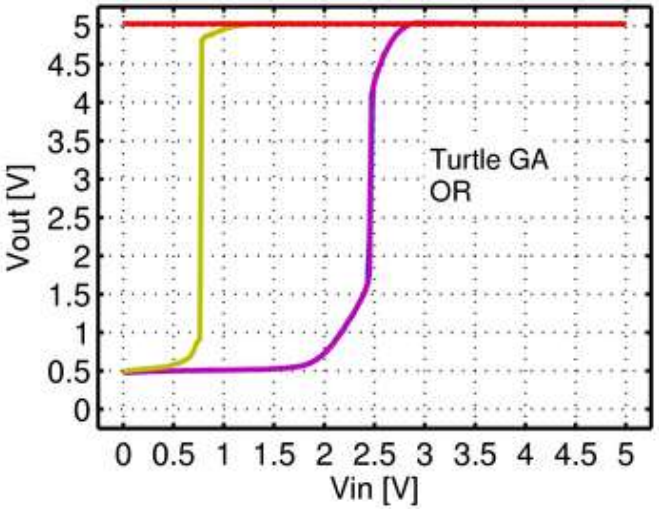


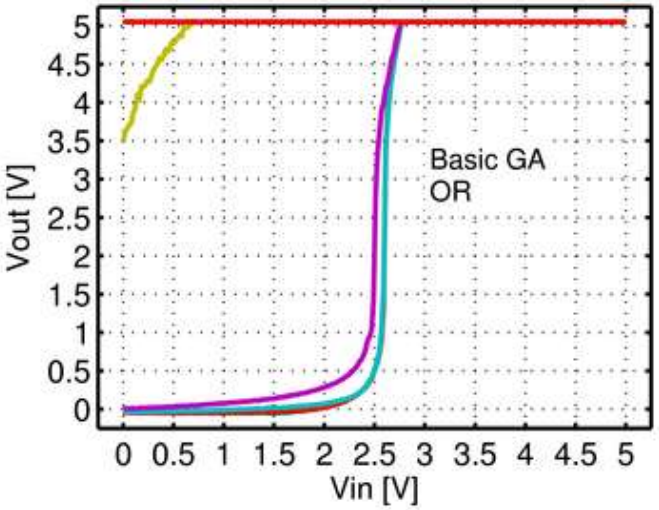


OR Gate : Comparison of Both GAs

- both algorithms find good solutions for the OR
- voltage characteristic looks equally well in both cases
- Turtle GA reduces resource consumption

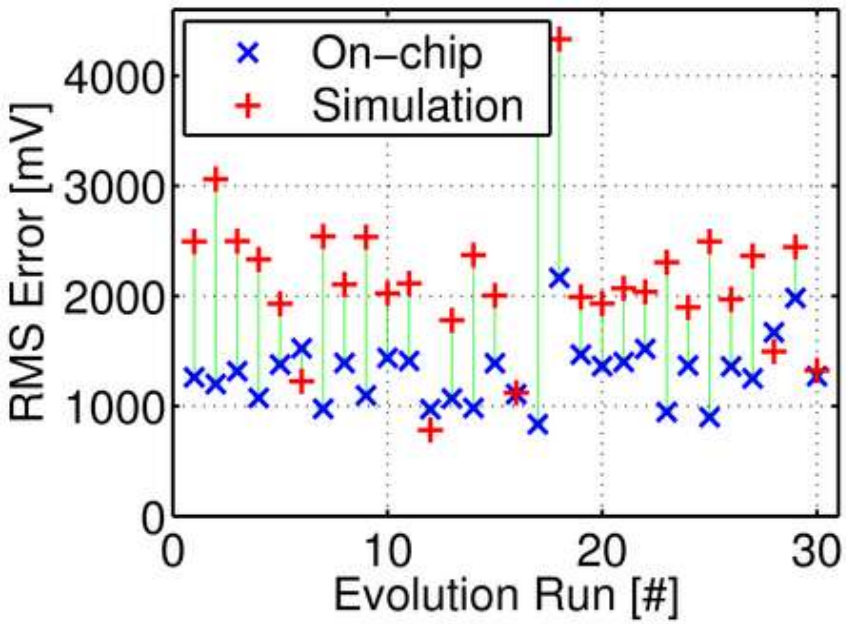


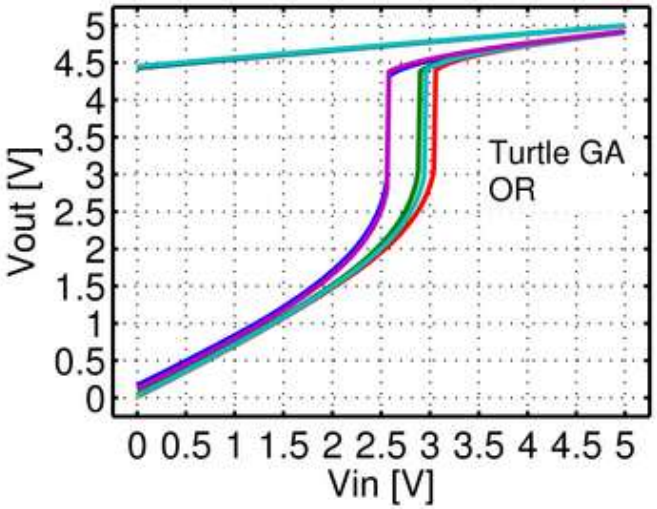




OR Gate : Simulation Results

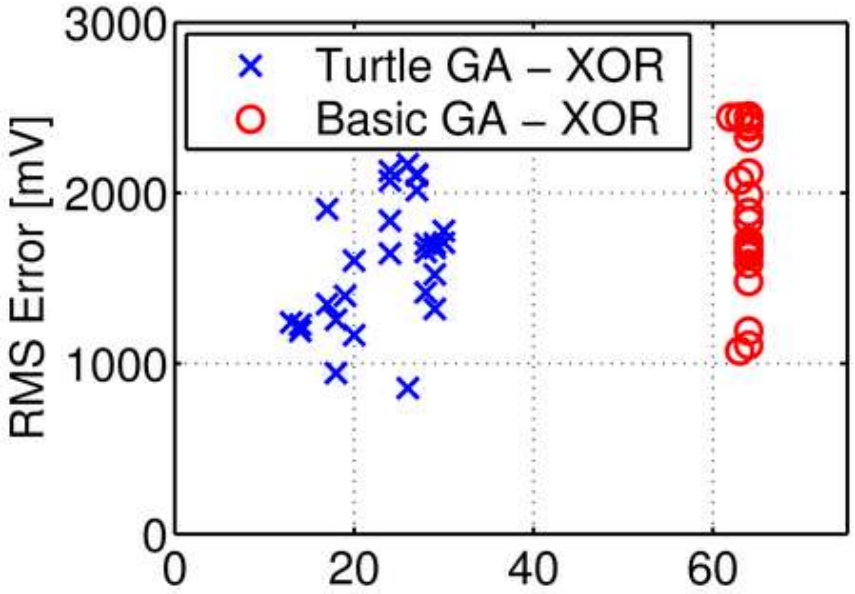
- most of the circuits perform worse
- the best solutions perform as well as on the FPTA

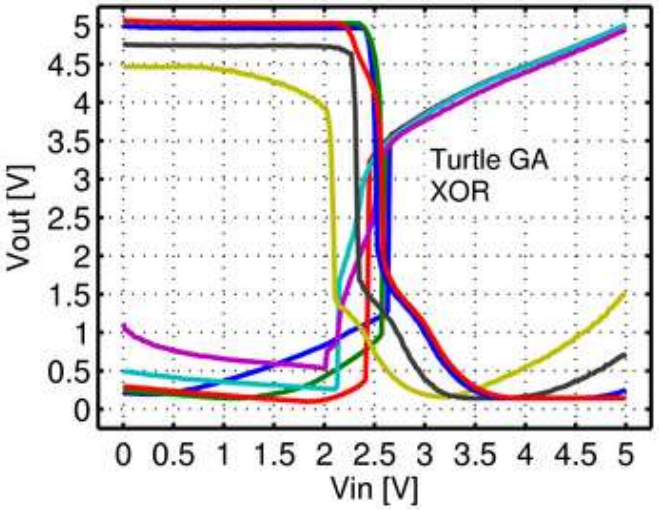


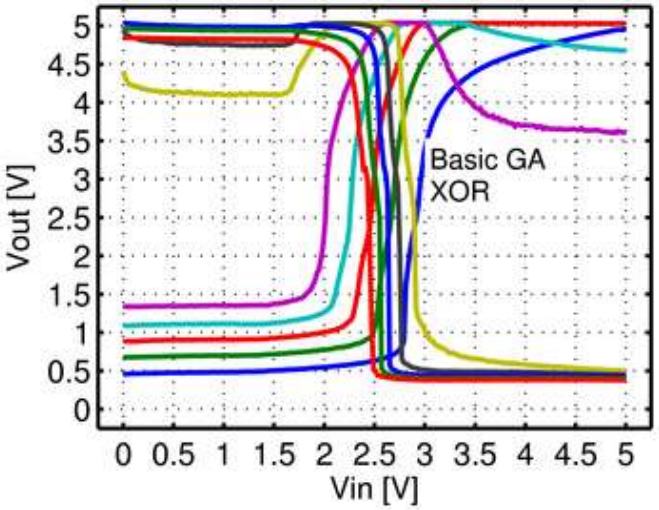


XOR Gate : Comparison of Both GAs

- both algorithms find good solutions for the XOR
- voltage characteristic looks equally well in both cases
- Turtle GA significantly reduces resource consumption

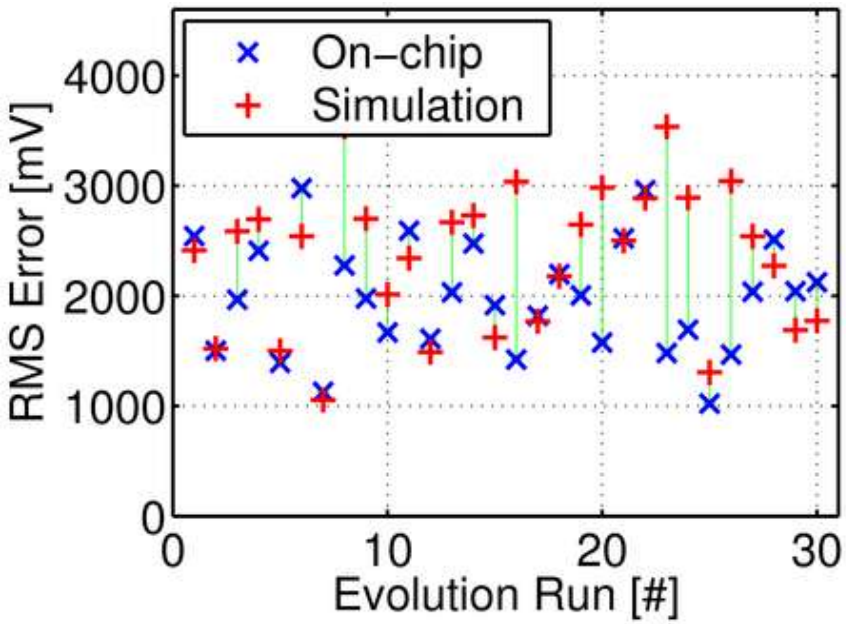


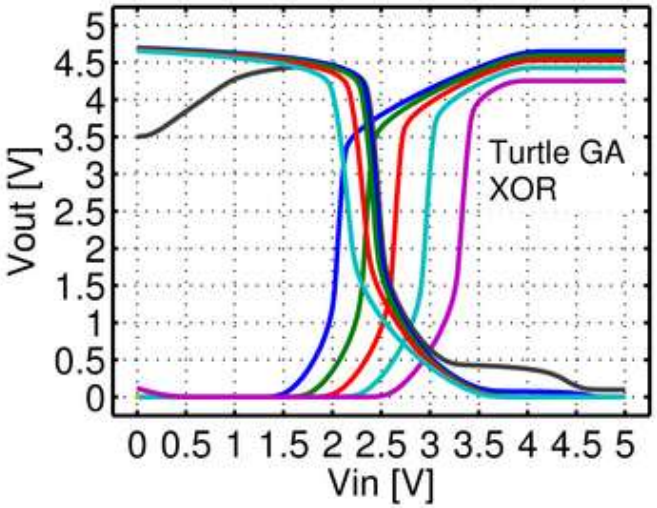




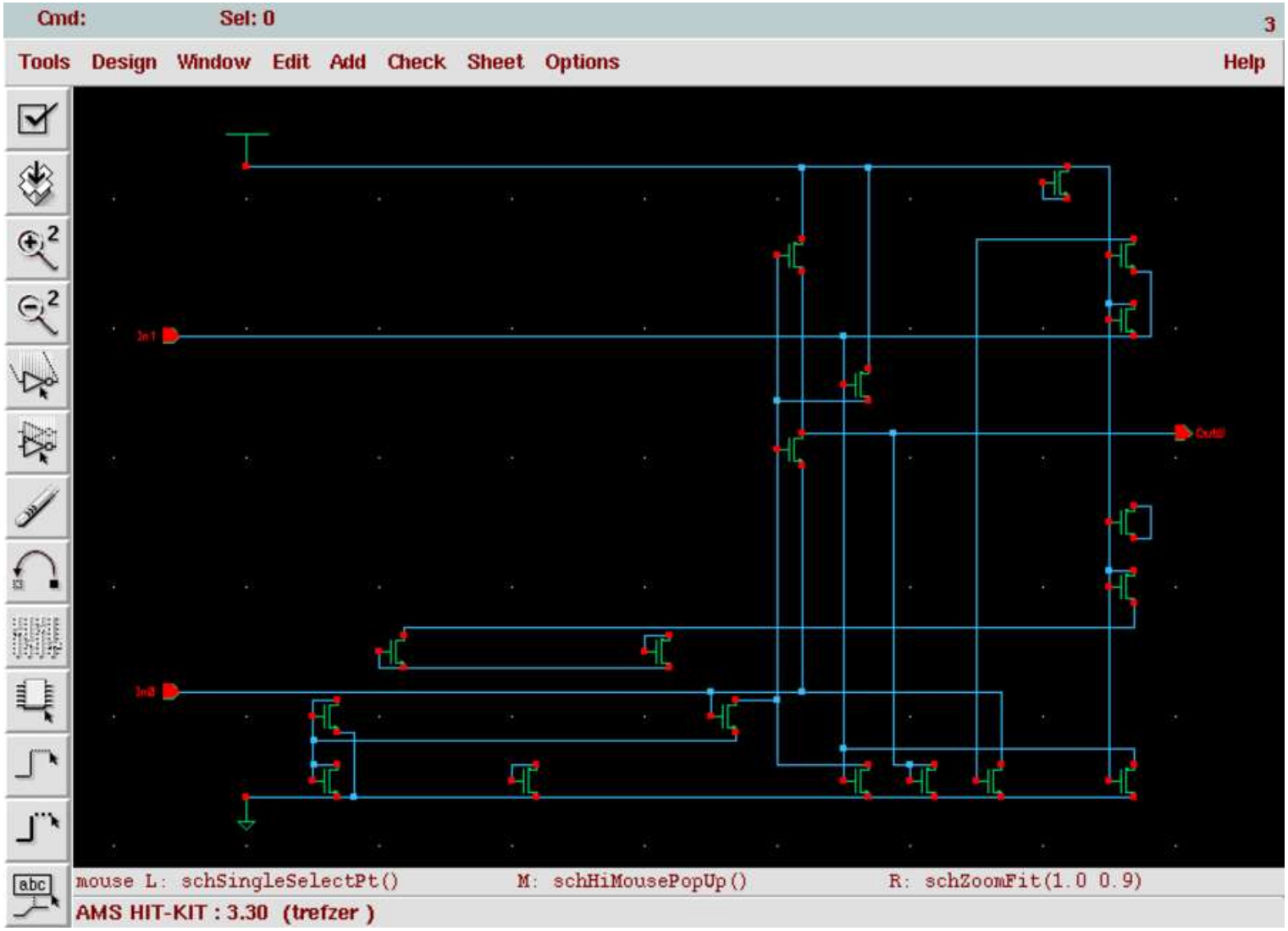
XOR Gate : Simulation Results

- the most difficult logic gate to evolve
- equal RMS errors in simulation and on the FPTA





Closing the Loop to Human Design

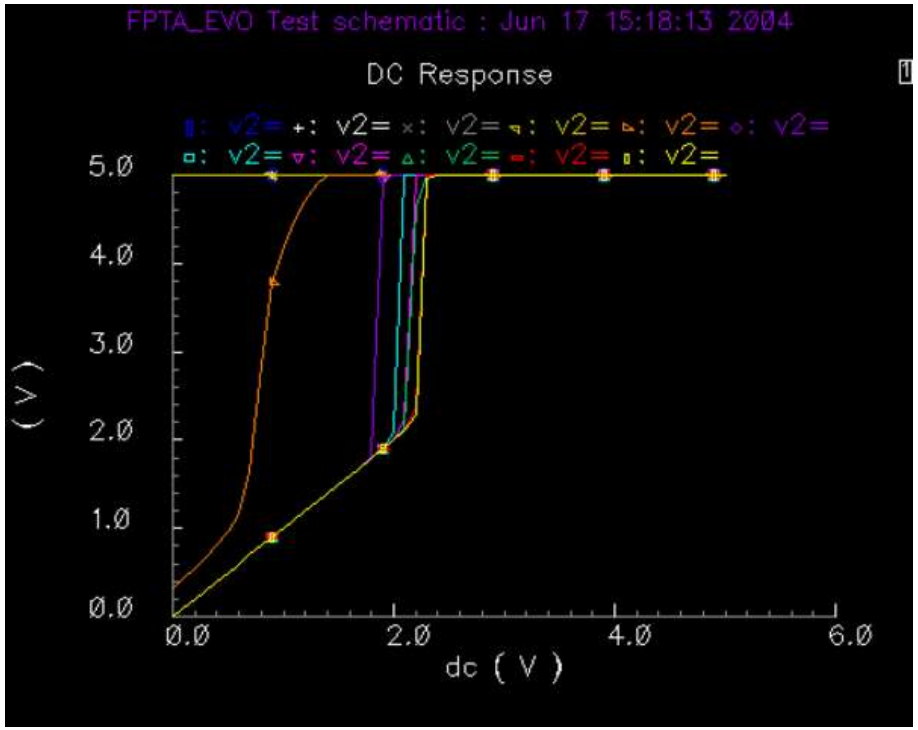


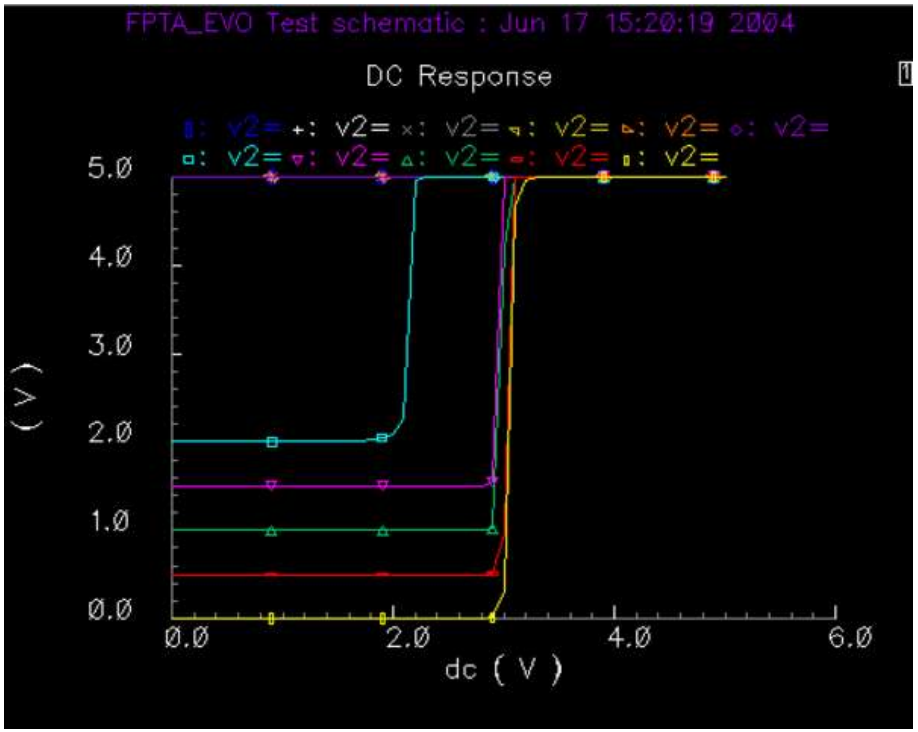
- transistors are sorted by gate (x) and drain (y) potential

Closing the Loop to Human Design

A promising result:

- the best evolved OR, converted to a human readable schematic
- good output voltage characteristic (+inversed inputs!)
- schematic and simulation: Cadence





Conclusion

Performance of the Turtle GA:

- Logic gates and comparators have been successfully evolved
- resource consumption (no. used transistors) is substantially reduced
- The best solutions perform well in both, simulation and on-chip measurement

Achievements:

- Floating nodes are inherently avoided using the new variation operators
- Circuits can be extracted into netlists and simulated outside the FPTA
- First Steps towards understanding evolved transistor circuits are taken by converting them to human readable schematics

Future work:

- The influence of the parasitic effects of the FPTA on the performance of evolution are further investigated to improve the quality of simulation and the transferability to other technologies
- To improve understanding of evolved circuits the conversion to human readable schematics will be developed